STUDIES ON THE FABRICATION OF VERTICAL INTEGRATED MEMS DEVICES(Dissertation_全文)

AUTHOR(S):

Oba, Masatoshi

STUDIES ON THE FABRICATION OF VERTICAL INTEGRATED MEMS DEVICES

MASATOSHI OBA

2010

Contents

Chapter 3
Design and fabrication of through-hole interconnection

Chapter 4
Design and fabrication of wafer-level bonding

General Introduction

Micro Electro Mechanical Systems (MEMS), which is also called micro-machine technology, has been receiving attention as a technology that produces small, highly integrated, and highly functional devices in response to increasingly advanced, sophisticated, and complicated industrial systems. Extensive research and development efforts for MEMS are being made all over the world. MEMS technology is now evolving from micrometer to nanometer-structures by making use of semiconductor production equipment which is rapidly advancing towards more elaborate sophistication and large diameters of wafers. Integration of semiconductor devices to electronic circuits is also progressing.

Observing the market trends, the MEMS market began with industrial pressure sensors, automotive pressure sensors, accelerometers, ink-nozzles for ink-jet printers, and movable micromirrors for projectors and is expanding into wider fields including mobile phones, communications, healthcare products, game machines, and other areas. In particular, low-g accelerometers and gyroscopes are required by the market, from detection of 1-axis, 2- or 3-axis can be detected on System-on-a-Chip (SoC), progress of those technology is remarkable, and accelerometers can be measured as well as acceleration (translational), tilt, shock and vibration.

Figure 1 shows the procession of the MEMS market, according to a survey by iSuppli, U.S.A. Despite the adverse effects of the Lehman Shock in late 2008, from which started a global recession, this survey forecasts that the MEMS market, will recover in 2010 and expand at an annual growth rate of 10%, strongly stimulated by demand for mobile phones and other mobile terminals as well as accelerometers and gyroscopes to be used in consumer electronics industry. As a result, the MEMS market, according to this survey, will, in 2009, exceed the past peak recorded in 2007 and the total market capitalization will reach US$ 8.5 billion in 2013 [1].

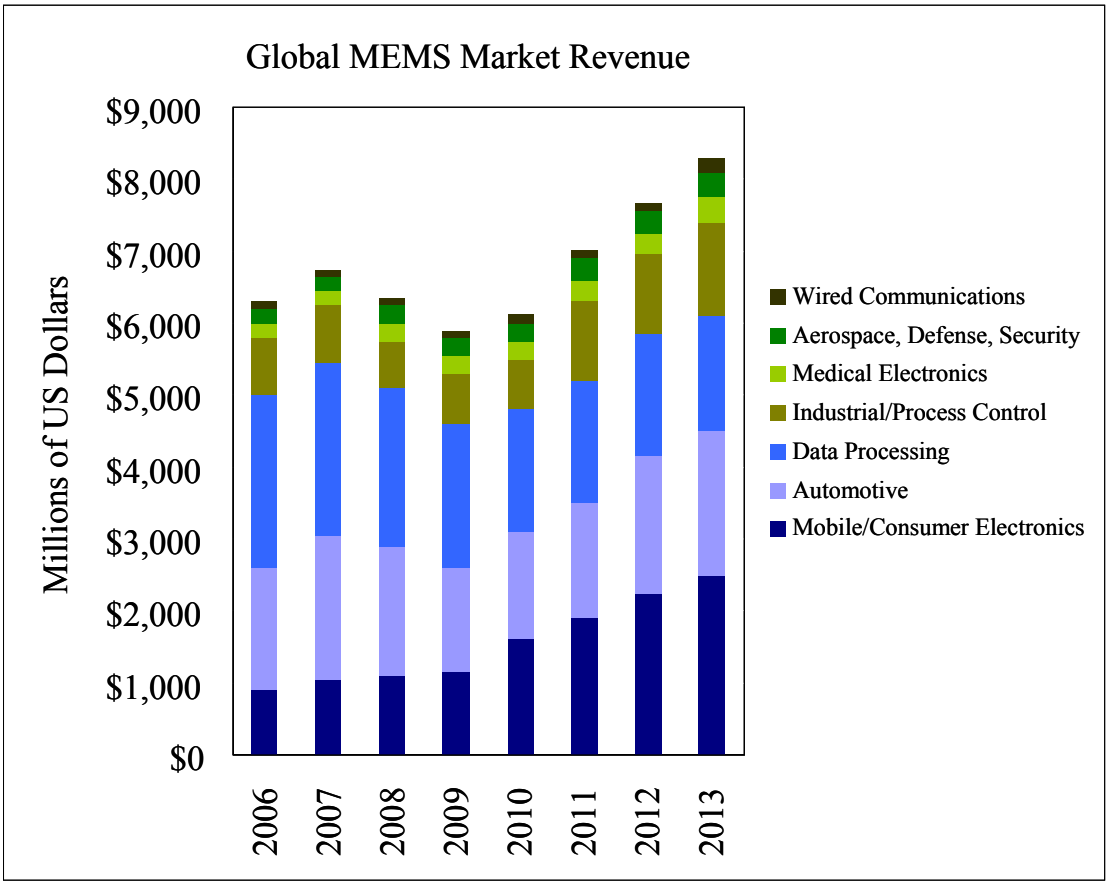


Fig.1 MEMS market changes from 2006 to 2013; Revenue will rise by 6.6 percent in 2010 and by 13.1 percent in 2011. Revenue will reach $6.99 billion in 2011, higher than the $6.7 billion in 2007. The global MEMS market will manage a Compound Annual Growth Rate (CAGR) of 10 percent from 2009 through 2013 [1].

Recently, infrared sensors that detect the presence of humans by sensing infrared rays emitted from the human body are receiving people's attention as one of the more popular MEMS devices, and are utilized from an energy saving viewpoint in home electric appliances such as air conditioners and Flat-Panel TVs.

It is expected that the infrared sensor applications is not limited to energy-saving functions, but also extended to safety and security fields, including the watching of senior citizens, due to functions used not only to detect the presence of humans, but also to obtain information on the positions and movements of humans as well as temperature distribution. For this purpose, infrared sensors must be assembled in arrays so as to detect lines and plane information, rather than mere spot information. In the field of the air conditioners in particular, the room-temperature distribution can be measured by automatically swinging plural infrared ray sensors which were able to line up lengthwise, room and person's situations are analyzed from the measured thermal imagery, and dehumidification and the change of air-conditioning are controlled according to the change in the outside temperature.

Unfortunately, existing infrared array sensors typically used for infrared cameras are very expensive. Therefore, the development of inexpensive infrared array sensors is demanded. As a high-definition infrared camera, CCDs (Charge Coupled Device) image sensors are able to take images of people by working with wavelengths close to infrared rays, however, such cameras are not sensitive enough as they have to use the active method of illuminating the target and receiving the rays reflected from the target. As such devices require an additional illumination unit, they still remain above the cost for general use.

The typical detection methods used for non-CCD infrared sensors are (i) pyroelectric, (ii) bolometric, (iii) thermopile, and (iv) diode methods [2-5]. If low cost is a concern, thermopile infrared sensors are suitable because they can be fabricated by Complementary Metal-Oxide Semiconductor (CMOS)

processes, which are used for Integration Circuit (IC) and Large-Scale Integration circuit (LSI) production. However, the thermopile method has a weak point in that its thermoelectric effect is lower than other methods and less sensitive. Increasing the number of thermopiles and expanding the size of the absorbing film to increase the aperture ratio might be used to increase the sensitivity [6-7]. These methods, however, will go against the principle of miniaturization.

On the other hand, MEMS technology is itself evolving from the use of silicon wafers as the main material used in the formation of structures through wet etching of bulk MEMS, to surface MEMS compatible with standard semiconductor processing and dry-etching of bulk MEMS. As a result, the fabrication of ultra-miniature precision devices is now possible. However, before the realization of smaller infrared array sensors, they need to be enclosed in standard TO-8 packages to be manufactured at lower costs. Since conventional side-by-side mounting methods and monolithic methods [8] involve the problem of an increase in mounting area, new MEMS device and IC mounting technology to further reduce the mounting area is demanded.

Though technologies for vertically integrating MEMS devices and IC are advancing to satisfying this demand, there remains the technological problem of how to achieve through holes with high aspect ratios in the MEMS device itself. Vertical integration technology, which is called Through-silicon via (TSV), is already been used for LSI and other semiconductor devices [9], and consists of wafer through-hole, through-hole interconnection, and wafer-level bonding technologies. In TSV technologies for semiconductor devices, the via or hole is etched through the silicon with many overlying layers of metal and dielectric using a deep reactive ion etching (DRIE) process. This hole is then typically lined with a dielectric deposited by chemical vapor deposition (CVD). Then, much as with copper dual damascene processes, a diffusion barrier and copper seed layer is deposited by physical vapor deposition (PVD), and the hole is filled by electroplated copper.

One of the main issues to consider in TSV processing is when and where it will be done, and there are two approaches. The first approach, called via-first, is to design it in at the start and then physically create the via before CMOS or LSI metallization. With via-first, the dimensions of the vias are typically smaller (from 5 to 20-μm diameter), with aspect ratios of 3:1 to 10:1. The other approach, called via-last, is to create the via after bonding, essentially when the wafer is finished. In this case, the processing can be done by the packaging house. The dimensions of the vias in this case are wider (from 20 to 50-μm diameter), with equally challenging aspect ratios of 3:1 to 15:1. Such aspect ratios are possible as the thickness of semiconductor wafers to be integrated can be reduced. In contrast, as MEMS requires wafers to be 2 to 3 times thicker than LSI and other semiconductor wafers, formation of as high-aspect-ratio as possible for such through-holes has been the issue to be addressed.

This study is concentrated to further reduce the size of thermopile infrared MEMS array sensors that can be fabricated by conventional CMOS processes. In general, sensor devices become less sensitive when they are made smaller. To compensate for this sensitivity reduction, infrared MEMS array sensor is performed research and development into micromirror arrays designed to concentrate infrared rays.

Additionally, a new technology is developed that integrates MEMS devices and IC vertically in order to minimize the area on which MEMS devices and IC are mounted. For this purpose, wafer through-hole formation, through-hole interconnection formation, and wafer-level bonding technologies are studied and the structural and electrical characteristics are assessed.

This thesis discusses the technological outcome of activities for developing a small, highly-sensitive, concentrated-infrared MEMS array sensor and integrating this infrared MEMS array sensor and IC vertically with high-aspect-ratio through-hole interconnections.

This thesis consists of four chapters. Essential elements and an overview

of each chapter are as follows.

Chapter 1 summarizes study themes and problems concerning infrared MEMS sensor technologies and identifies problems to be solved for ultra miniaturization required for a 16 x 16 array. The sensitivity of each device must be increased to achieve ultra miniaturization. A reflecting structure with silicon micromirrors formed is proposed and its fabrication process is described. Also, in order to improve the sensitivity of an infrared MEMS sensor, the effect of the vacuum at thermal insulation is verified. In addition, the necessity and innovativeness of high-aspect-ratio through-hole formation technology are described because this technology is indispensable for vertical integration of MEMS and IC wafers and is considered as a method that allows ultra-miniature infrared MEMS array sensor to be mounted in small TO-8 packages.

Chapter 2 summarizes the present status and problems of studies concerning vertical integration MEMS technologies and describes the possibility of solving these problems. The technological problem to be solved for vertical MEMS integration is how to form high-aspect-ratio through-holes. Vertical integration technology is also been used in LSI and other semiconductor devices, but an aspect ratio range from 5 to 15 is satisfactory. This is because semiconductor wafers can be thinned. Thinning is done by grinding, chemical mechanical planarization (CMP) or by a wet chemical process.

In contrast, MEMS requires the use of wafers that are 2 to 3 times thicker than LSI and other semiconductor wafers. This raises the problem of how to form higher-aspect-ratio through-holes. This thesis describes a new technology that can form through holes with a 5-μm diameter and 50:1 aspect ratio and summarizes the characteristics and issues that are found to form an insulation layer using Tetraethyl Orthosilicate (TEOS) oxide film.

Chapter 3 discusses the technology that forms electric interconnections in through-holes with a 5-μm diameter and 50:1 aspect ratio. The

interconnection formation methods described in this chapter include the Cu bottom-up plating method which can be used after the formation of the MEMS structure and the doped poly-Si interconnection formation method which can be used in a relatively early stage of the MEMS process.

The major challenge in the bottom-up plating method is the formation of an interconnection layer (seed layer) from which plating grows. To accomplish this task, a new jig is created to be used to form the seed layer. This method proved to be useful for practical interconnection formation. These interconnection formation processes and conducted electrical conduction tests are assessed to demonstrate that this interconnection formation method was satisfactory for vertically integrated interconnections.

Since the doped poly-Si interconnection formation method is advantageous in that it can be used in an early MEMS process stage with relatively short lead time, the interconnection formation process based on this method and conducted electric conduction tests are also assessed.

Chapter 4 discusses wafer-level bonding. It includes the proposal of concurrent bonding technology for hermetic sealing and electric connection that can be used to bond three or more IC and MEMS wafers. This chapter also covers data on the three-layer bonding alignment accuracy and the leak rate found by hermetic sealing tests to demonstrate that the hermetic sealing achieved is at a level of practical use. The results of electric conduction tests performed on a three-layer laminated structure including IC and through-hole interconnections are also included. Infrared MEMS array sensor can be fabricated by the results of this chapter as the technology that can achieve the structure of hermetic sealing, and infrared MEMS array sensor wafer and IC wafer can be bonded by using vertical integration technology at the wafer-level bonding.

Summary describes the outcome of this study and concludes this thesis in terms of presenting future perspectives.

References

[1] “Global MEMS Market Suffers First-Ever Decline in 2008”, http://www.isuppli.com/News/Pages/Global-MEMS-Market-Suffers-First-Ever-Decline-in-2008.aspx, iSuppli Corp., April 29, 2009

[2] C.M.Hanson, H.R.Beratan, and D.L.Arbuthnot, Proc. SPIE, Vol.1735, **17**, 1992

[3] R.A.Wood, C.J.Han, and P.W.Kruse, Tech. Digest of IEEE Solid-State Sensor and Actuator Workshop, **132**, 1992

[4] M.Hirota, T.Ohta, and Y.Fukuyama, Proc. SPIE, Vol.6940, **694032-1**, 2008

[5] Y.Kosasayama, T.Sugano, Y.Nakaki, Y.Fujii, H.Inoue, H.Yagi, H.Hara, M.Ueno, M.Takeda, and M.Kimata, Proc. SPIE, Vol.5406, **504**, 2004

[6] Y.Ohta, Y.Arakawa, T.Fukumoto, Y.Fukuyama, and M.Hirata, Proc. the 26th Symposium on Sensors, Micromachines & Applied Systems, **622**, 2009

[7] T.Ishikawa, M.Ueno, K.Endo, Y.Ohta, J.Nakanishi, K.Kasasayama, H.Yagi, T.Sone, and M.Kimata, Proc. SPIE, Vol.4130, **152**, 2000

[8] W.Kuehnel and S.Sherman, Sensors and Actuators A, vol.45, No.1, **7**, 1994

[9] M.Kawano, S.Uchiyama, N.Takahashi, Y.Kurita, M.Komuro, and S.Matsui, IEEE Transaction on Electron Devices, Vol.55, Issue.7, **1614**, 2008

Chapter 1

Design and fabrication of high-sensitive infrared MEMS array sensor

1.1 Introduction

Recently, technologies that dramatically increase optical sensitivity and thermal insulation efficiency have been developed and are used for uncooled infrared sensors, which detect the presence of humans by sensing infrared rays emitted from the human body and are utilized from an energy saving viewpoint, in home electric appliances such as air conditioners and Flat-Panel TVs.

The characteristics of these infrared sensors include:

(a) No illumination required,
(b) Temperature information can be obtained,
(c) The sensor is not susceptible to smoke or fog,
(d) The contrast between the human body and the background is clear,
(e) No shadow is produced, and
(f) The sensor does not require a cooling unit because it is small and consumes low power.

It is expected that the infrared sensor applications is not limited to energy-saving fields, but also extended to safety and security fields, including the watching of senior citizens, due to functions used not only to detect the presence of humans, but also to obtain information on the positions and movements of humans as well as temperature distribution. For this purpose, infrared sensors must be assembled in arrays so that they can detect line and plane information, rather than mere spot information. In the field of the air

conditioners in particular, the room-temperature distribution can be measured by automatically swinging plural infrared sensors which were able to line up lengthwise, room and person's situations are analyzed from the measured thermal imagery, and dehumidification and the change of air-conditioning are controlled according to the change in the outside temperature. Unfortunately, existing infrared array sensors typically used for infrared cameras are very expensive. On the other hand, since a pyroelectric type infrared sensor consists of same piezoelectric ceramic materials as used capacitors, actuators [1], and other sensors, and is excellent in mass production, it is inexpensive, but only an infrared changed portion is detectable. In addition, mechanical components such as microminiature motor [2] to swing the plural infrared sensors automatically are also necessary, and the cost increase. Therefore, the development of inexpensive infrared array sensors is demanded.

The typical detection methods used for infrared sensors are (i) thermopile, (ii) pyroelectric, (iii) bolometric, and (iv) diode methods. Figure 1.1 shows a classification of the detection methods for infrared sensors. If low cost is a concern, thermopile infrared sensors are suitable because they can be fabricated by CMOS processes, which are used for IC production.

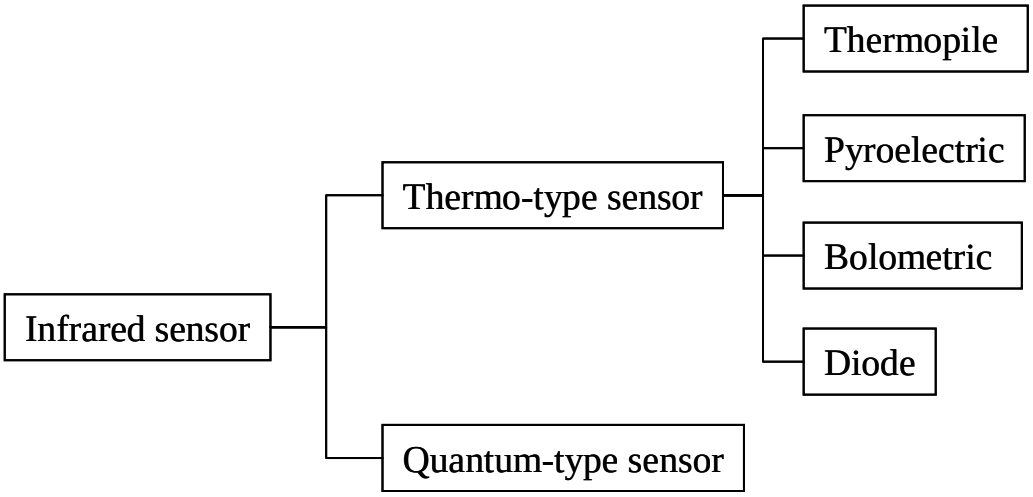


Fig.1.1 Detection methods for infrared sensors.

The bolometer type [3], an infrared sensor, Honeywell announced in 1992, as shown in Figure 1.2. A bolometer film is formed to the bridge structure by using the surface micromachining technology on IC substrate, and an excellent structure in productivity. However, there is a problem in the reliability of the bolometer film. The reflective film in the figure seems to work not only by reflecting infrared rays coming from above the bolometer, but also preventing heat dissipated from the IC from transmitting to the bolometer. Although the bridge structure helps increase the heat insulation efficiency, the cavity formed between the bridge and the substrate using sacrificial layer etching does not provide sufficient heat insulating properties due to difficulty in increasing the separation distance from the IC.

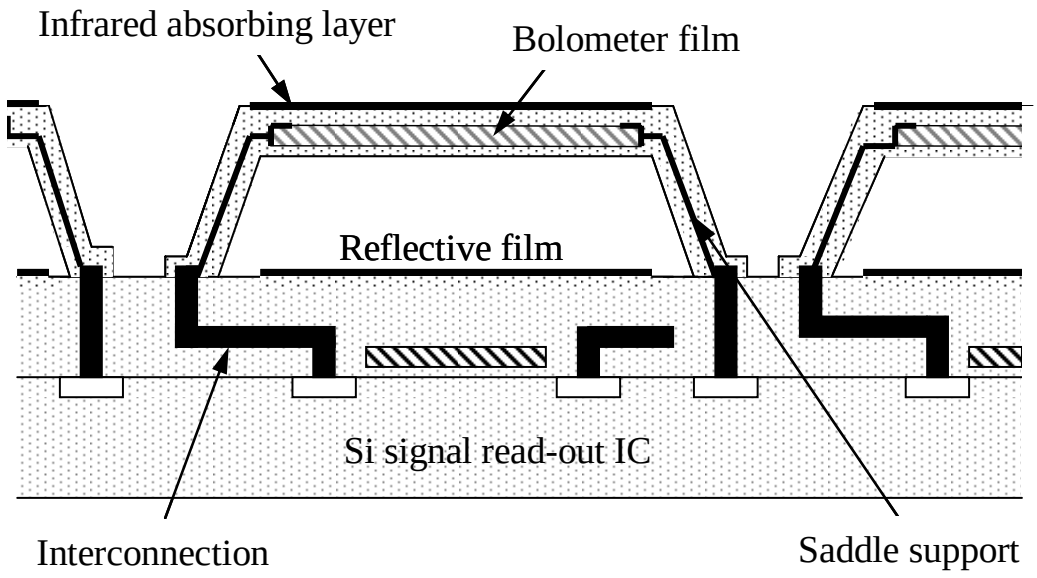


Fig.1.2 Bolometer type infrared sensor.

The silicon-on-insulator (SOI) diode type [4], an infrared sensor, Mitsubishi Electric Co. announced as shown in Figure 1.3. This sensor includes diodes mounted on the SOI active layer as temperature sensors to ensure that it emits low noise. The infrared absorbing layer connected to the

diodes absorbs infrared rays efficiently and the reflective film formed by the bottom metal film improves the absorption efficiency. Its aperture ratio, which is an index of sensor sensitivity, is very large, but too large an infrared absorption layer will increase the thermal time constant that governs transmission of absorbed heat to the diode which may decrease the response frequency. In addition, the construction in which etching stoppers of a trench structure are provided on the silicon substrate so that they will be used as the side walls when the substrate cavity is isotropically etched with XeF_6 seems to be a hampering factor for mass-production.

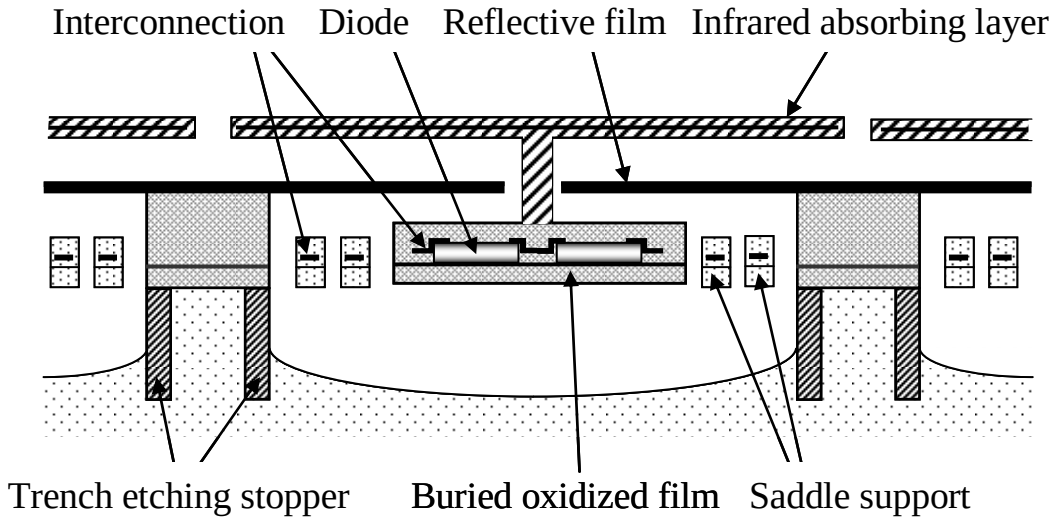


Fig.1.3 SOI diode type infrared sensor.

The thermopile method [5] is a sensor connecting different conductors in series as shown in Figure 1.4. As semiconductors have larger Seebeck coefficients than metals, by connecting p-type and n-type semiconductors whose Seebeck coefficient signs are opposite will allow for higher productivity of infrared sensors. However, the thermopile method has a weak point in that its thermoelectric effect is lower than other methods and less

sensitive. Though methods to increase sensitivity are being developed by increasing the aperture ratio through an increase of the number of thermopiles or expanding the size of the absorbing film [6-7], they go against the principle of miniaturization.

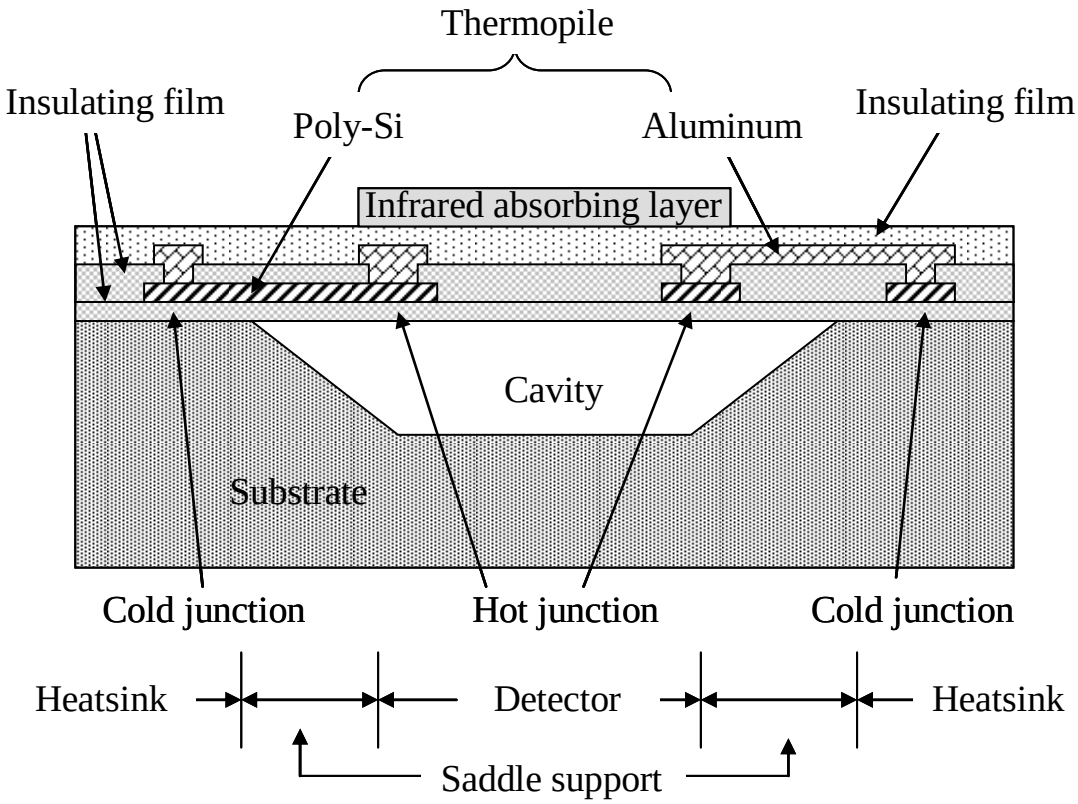


Fig.1.4 Thermopile type infrared sensor.

For materializing small and inexpensive infrared array sensors, micromirror arrays was developed to concentrate infrared rays, in order to compensate for the decreased sensitivity by the miniaturized elements, using thermopile infrared array sensors that can be made using CMOS processes. Then infrared array sensors ware verified the effects of micromirror arrays for improvement of sensitivity through simulations and actual measurement based on the evaluation results.

1.2 Structure of infrared MEMS array sensor

Figure 1.5 shows a cross-sectional schematic of the infrared MEMS array sensor.

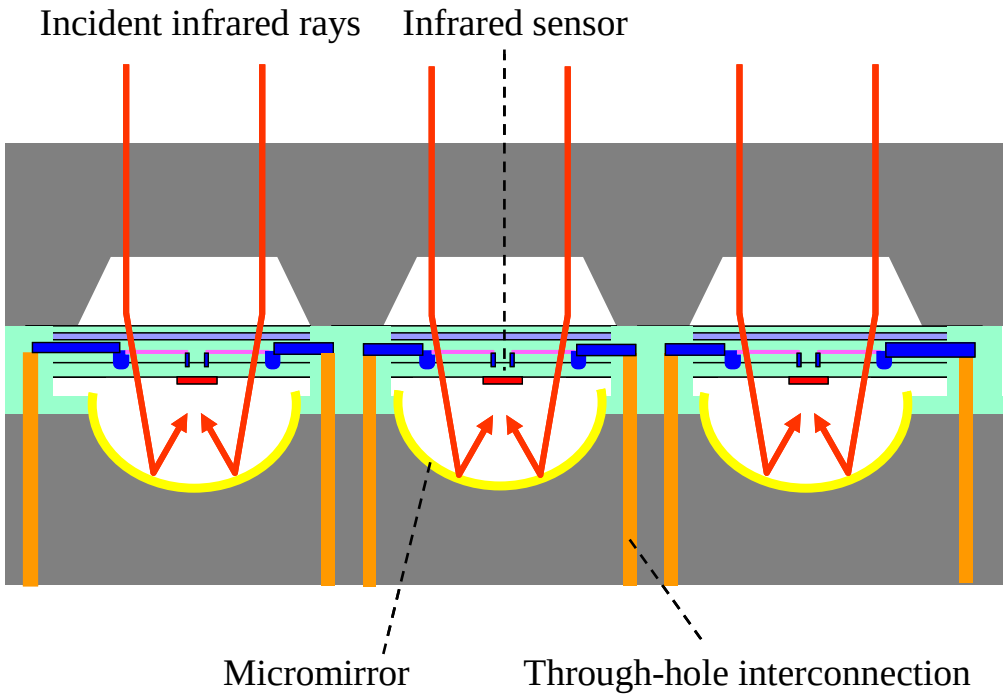


Fig.1.5 Cross-sectional schematic of the infrared MEMS array sensor.

The infrared MEMS array sensor is structured so that incident infrared rays from above the sensor are reflected and concentrated by the micromirror array at the bottom, and then re-enter the infrared sensor at the top, this time, on the infrared absorbing film. This structure makes it possible to increase the aperture ratio of the infrared MEMS array sensor and increase the amount of infrared rays entering the infrared absorbing film. This leads to an improvement in sensitivity. In addition, since the infrared sensor arrays and the micromirror arrays are each fabricated on silicon substrates, these devices can be bonded to be sealed hermetic. Therefore, it is possible to further

improve the heat insulation properties through reduction of internal pressure, thereby further improving the infrared sensor sensitivity.

1.2.1 Design and process of 16 x 16 infrared MEMS array sensor

Figure 1.6 shows a top view of the infrared sensor. Thermopiles are formed on the thin membranes extending from the four corners and the infrared absorbing film is located at the center of the sensor. Hot junctions are formed on the thin membranes, and cold junctions are formed on the thick silicon rim. The membrane structure is formed using anisotropic wet etching applied through four etching holes. And Figure 1.7 shows the infrared sensor array consists of these sensors arranged in a 16 x 16 array.

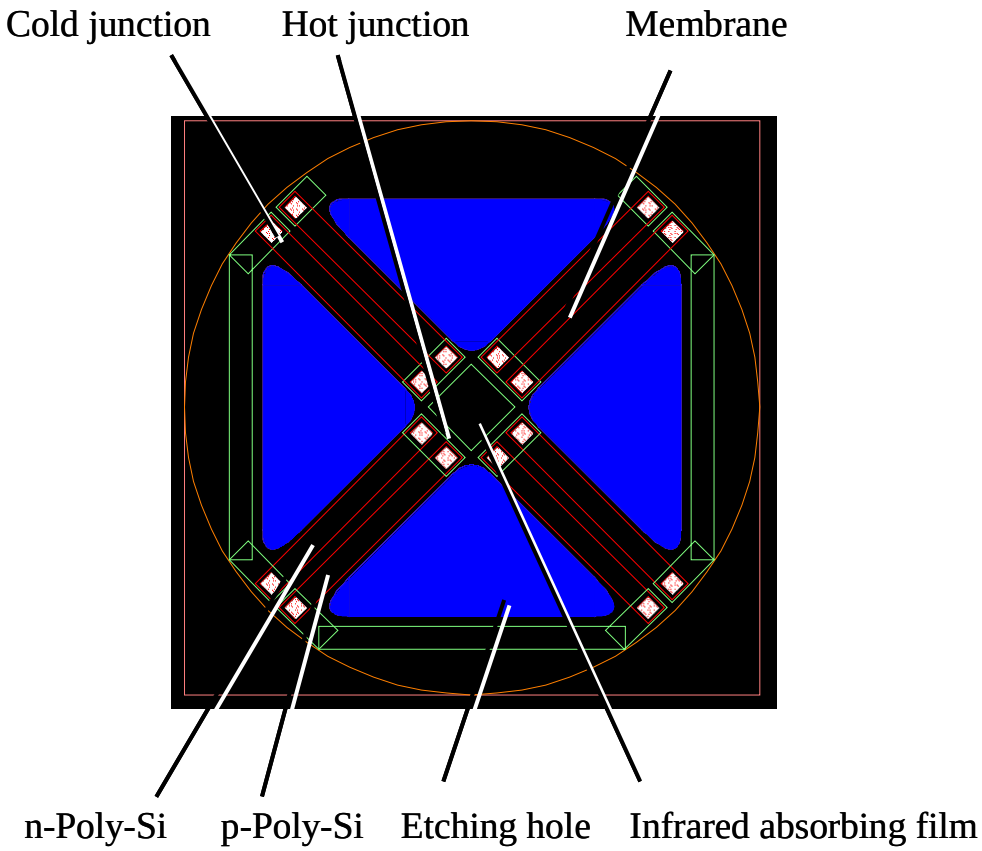


Fig.1.6 Top view of infrared sensor.

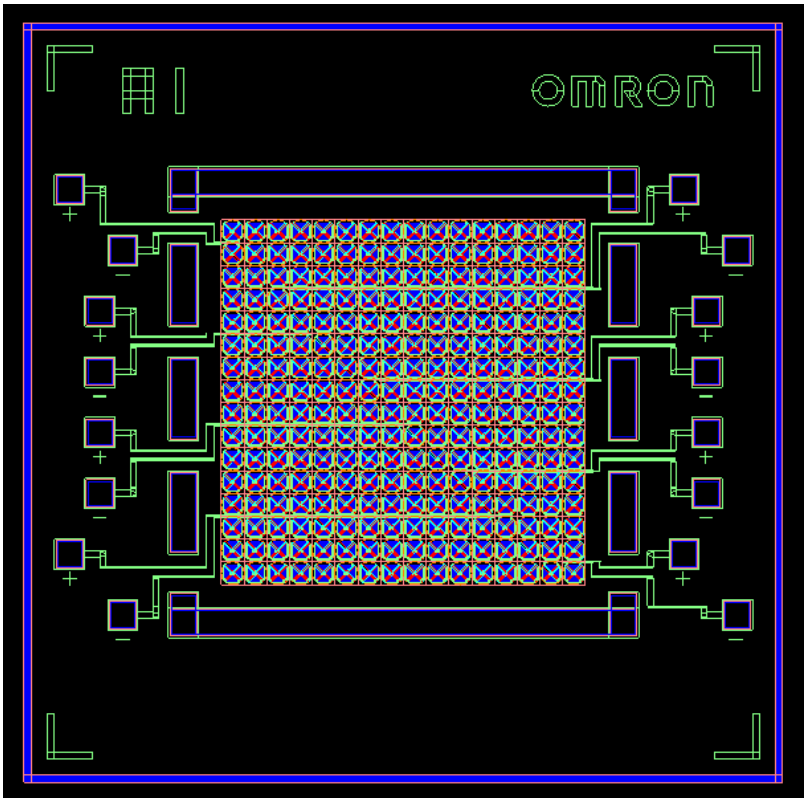


Fig.1.7 Layout design of infrared MEMS 16 x 16 array sensor.

Figures 1.8 (a) to (g) show the process flow of this infrared sensor, and fabrication process is as follows.

(a) Formation of dielectric membrane (1): On (100)-plane double-side -polished single crystal silicon substrate, 0.20-μm-thick thermally oxidized film and 0.25-μm-thick silicon nitride (SiN) film are formed on the silicon substrate by using a low pressure chemical vapor deposition (LPCVD) method. The silicon nitride is removed at the etching holes by dry etching. The silicon substrate is etched utilizing the etching holes by the anisotropic etching method using Tetramethyl ammonium hydroxide (TMAH) solution, and the membrane is formed.

(b) Formation of dielectric membrane (2): 0.14-μm-thick non-doped silicate glass (NSG) is formed by the LPCVD method, then it becomes 0.10-μm-thick by densification treatment to reduce stress.

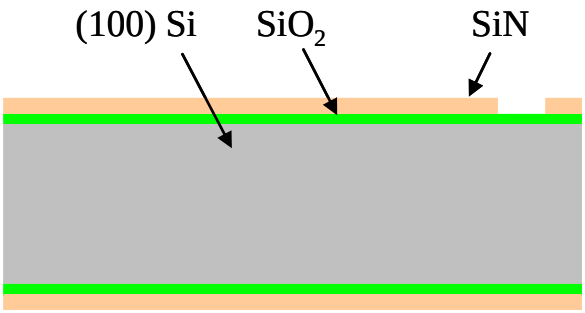
(c) Formation of poly-Si interconnection: 0.50-μm-thick poly-Si is formed by the LPCVD method, and phosphorus (P) ions and boron (B) ions are doped onto the individual thermopile parts. Then the surface is activated by an annealing process after patterning, and n-type and p-type poly-Si interconnections are formed. The oxidized film formed on poly-Si is removed by using a hydrofluoric acid (HF) solution, contact holes are formed.

(d) Formation of Al interconnection: 0.20-μm-thick aluminum (Al) is formed by sputtering, n-type and p-type poly-Si interconnections are connected and thermopiles are formed.

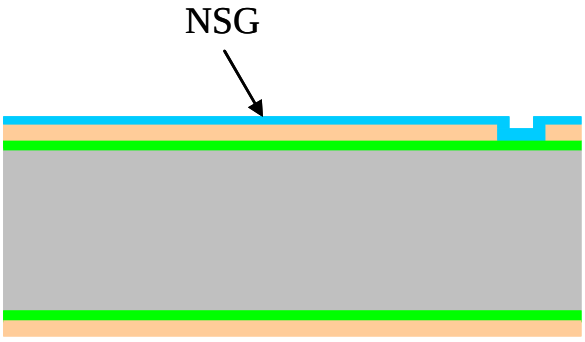
(e) Formation of dielectric membrane (3): 1.5-μm-thick NSG film is formed by the plasma-enhanced CVD (PECVD) method, 0.01-μm-thick titanium (Ti) film is formed by vacuum deposition as the infrared ray absorbing film, NSG film is formed by PECVD method, and these films are removed to form etching holes by dry etching and HF solution.

(f) Formation of Au/Cr: 0.10-μm-thick chromium (Cr) film and 0.50-μm-thick gold (Au) film are formed as the wire bonding pad, by vacuum deposition, then these films are treated by wet etching using a potassium iodide (KI) solution and a potassium ferrocyanide solution.

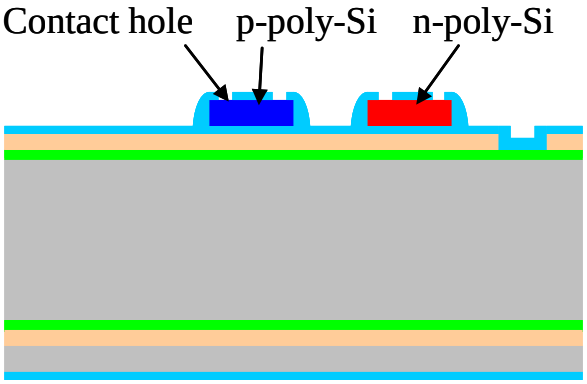
(g) Anisotropic etching: The oxidized film is removed on the etching holes and the silicon substrate under the membrane is etched by wet etching using a TMAH solution.



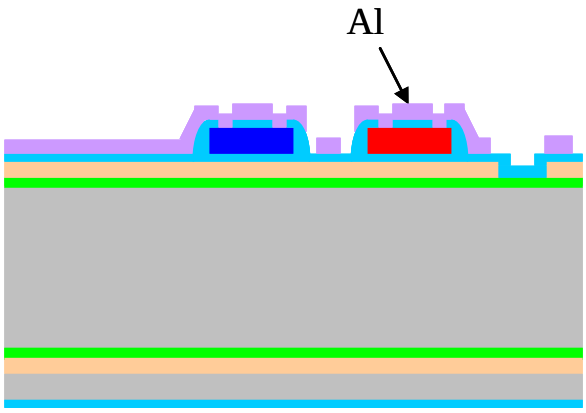
(a) Formation of dielectric membrane (1)



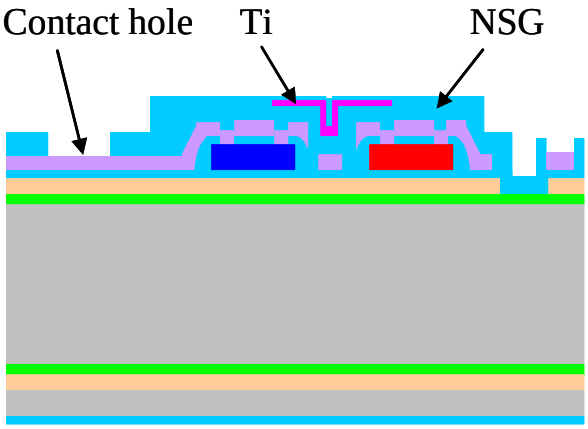
(b) Formation of dielectric membrane (2)



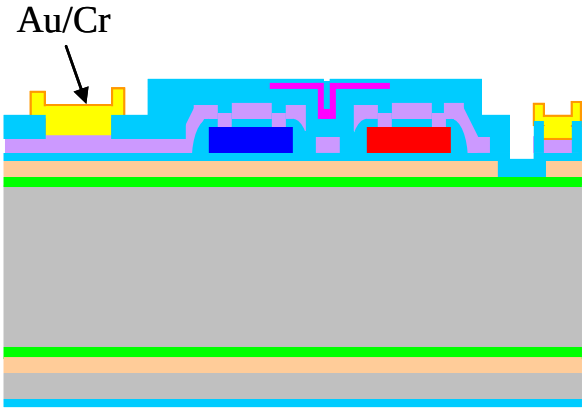
(c) Formation of poly-Si interconnection



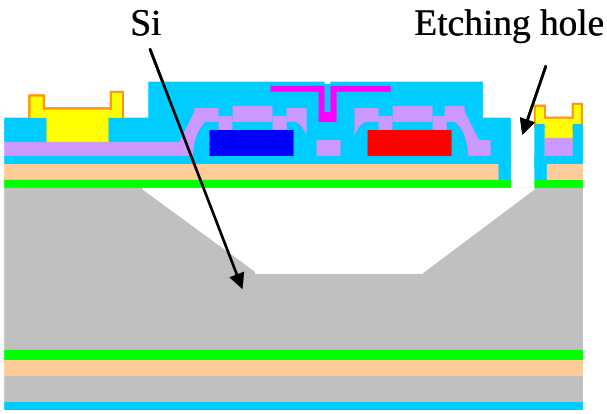
(d) Al interconnection formation



(e) Formation of dielectric membrane (3)



(f) Au/Cr formation



(g) Anisotropic etching

Fig.1.8 Schematic of infrared sensor process flow.

According to the process described above, infrared sensor was fabricated. Figure 1.9 shows a SEM photograph of the infrared sensor and Figure 1.10 shows a SEM photograph of infrared MEMS 16 x 16 array sensor.

The infrared sensor element is formed from four thermopiles pairs connected to the clockwise rotation in series. One thermopile consists of n-type poly-Si and p-type poly-Si, and is connected with Al interconnection. Voltage produces a thermopile in a difference of temperature by the Seebeck effect. Al interconnections are located on the thin membranes with small thermal capacity (cold junction) the thick silicon rim with large thermal capacity (hot junction) so that the difference of temperature by infrared rays may become large. Since such high voltage that the difference of temperature of the cold junction and the hot junction is large is obtained, it becomes high sensitivity.

This infrared sensor was designed as processing rule of poly-Si line width at 6 μm, the space at 4 μm and distance between the ends of the thin film at 4 μm, the bridge width becomes 24 μm,

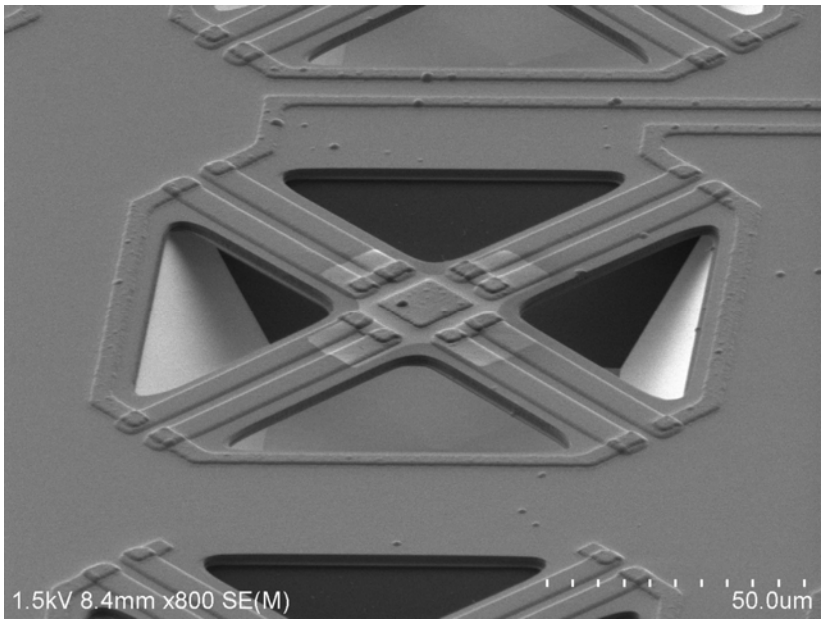


Fig.1.9 SEM photograph of Infrared sensor.

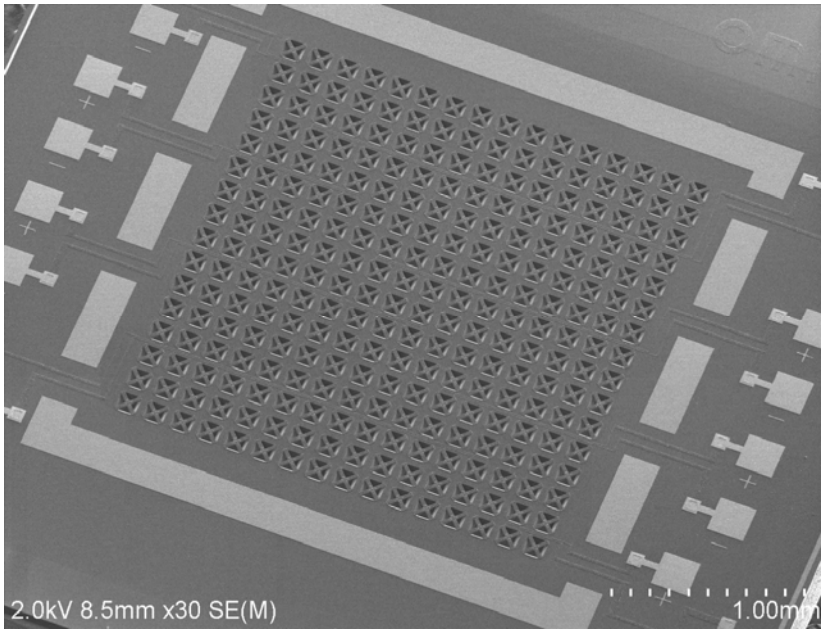


Fig.1.10 SEM photograph of infrared MEMS 16 x 16 array sensor.

1.2.2 Design and process of micromirror array

To make a curved form on the silicon substrate, the following method is used;

(i) holes are made with different depth as a base to make a curved form utilizing the RIE lag effect of deep reactive iron etching (DRIE), and (ii) the surface is smoothed by the dry etching method using SF_6 and other materials. Figure 1.11 shows a micromirror array process flow.

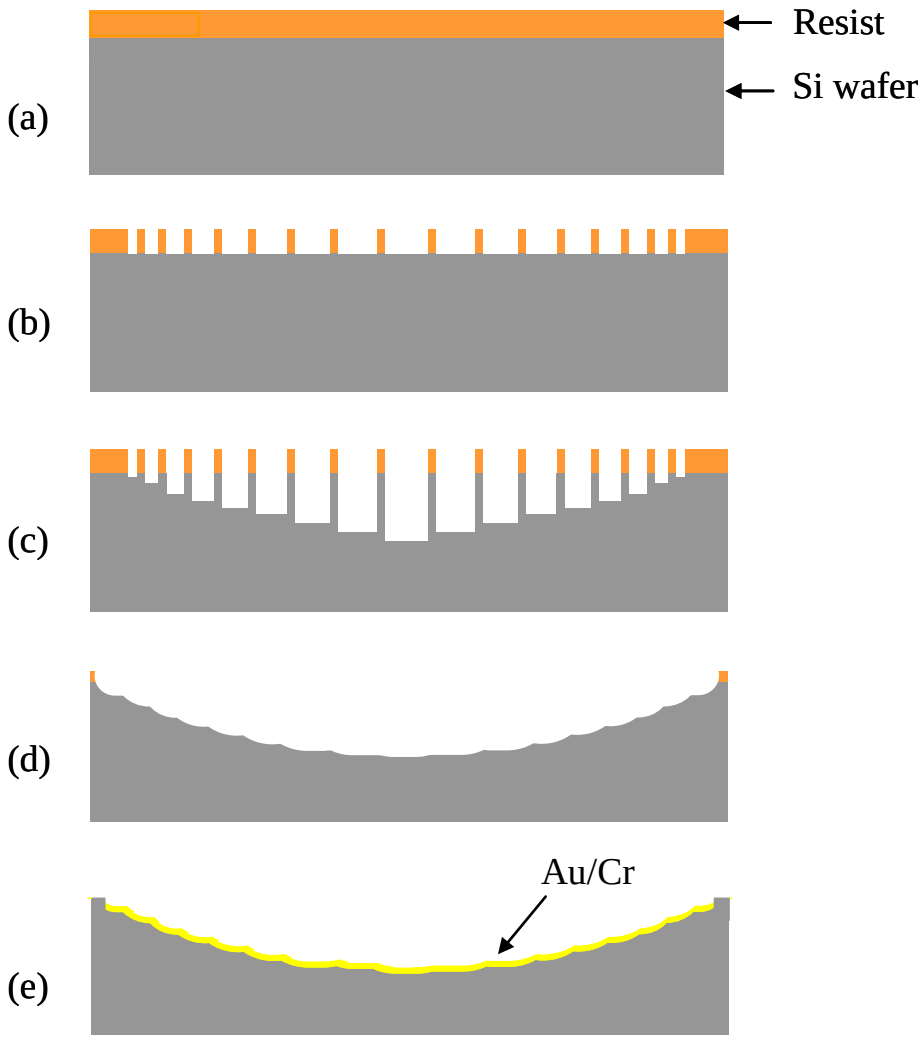


Fig.1.11 Cross-sectional schematic of micromirror array process flow.

The fabrication process of micromirror array is as follows.

(a) Coating a resist on the silicon wafer.
(b) Patterning the resist.
(c) Vertical etching by DRIE. (etching time: 360s)
(d) Removing the side walls of trenches and smoothing the surface by isotropic dry etching. (etching time: 400s)
(e) Formation of Au/Cr deposition on the micromirror array. (2-μm-thick Au / 0.5-μm-thick Cr)

By the research of T.Ohori, the University of Tokyo [8], the author used the electron beam (EB) lithography method for the fabrication of a concave lens structure, but in this study, a patterning method was selected using standard mask aligner taking into consideration the efficiency required for mass production [9].

In designing micromirror array, consideration about the following items is required.

- Relationship between mask opening and DRIE etching depth.
- Relationship between isotropic dry etching and surface roughness.
- Relationship between DRIE etching depth and isotropic dry etching depth.

Figure 1.12 shows the relationship between the mask opening area and the DRIE etching depth. The distance between the mask opening width and the mask opening was set at 2 μm, which is the minimum line and space that a standard mask aligner can expose. Therefore, the minimum mask opening area becomes 2 μm x 2 μm = 4 μm^2. The relation of etching depth (d) to opening area (S) proved to be: $d = 3.22 \log S + 13.68$.

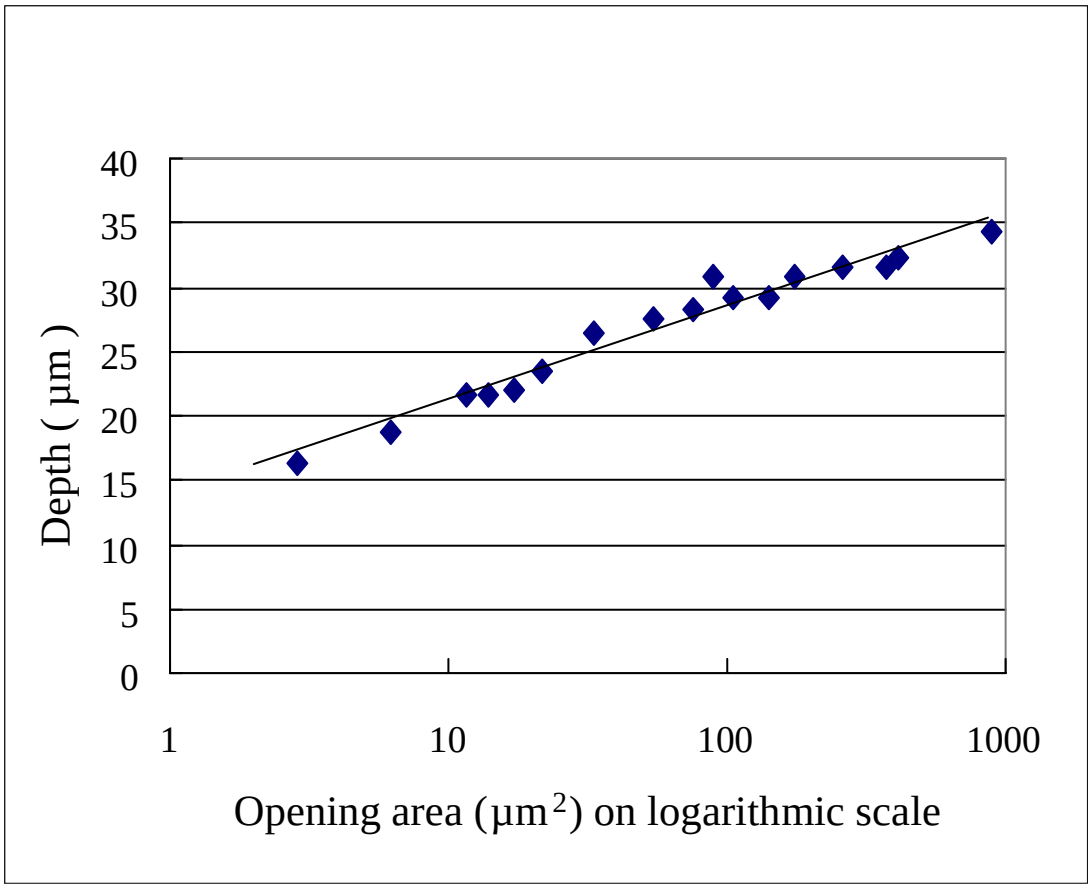


Fig.1.12 Relation between opening area and DRIE etching depth; The relation of etching depth (d) to opening area (S) proved to be: $d = 3.22 \log S + 13.68$.

The required conditions for surface roughness provided by isotropic dry etching were determined as follows:

The surface roughness target was set at Ra = 100 nm, by converting the mirror surface roughness in visible light at 5nm to the wavelength of infrared rays at 10 μm. If the isotropic dry etching time is short, the side walls shown in Figure 1.11(c) will not be sufficiently etched and a rough surface will be formed.

As a result of evaluation of surface roughness, the surface roughness will be Ra = 30 to 80 nm, which is small enough to achieve the target, when the isotropic etching rate is set at 0.3 μm/sec and the etching time at 400s.

Then etching quantity was calculated by measuring the difference in depth after isotropic dry etching and the depth after DRIE etching treatment. After comparison of the depth of mask opening areas of 4 μm^2 and 100 μm^2, the depth at 4 μm^2 proved to be 2.9 μm deeper than that of 100 μm^2. This is considered to be a result of excess etching, as a smaller opening area makes a shallower hole and causes the smaller Si side walls to be etched more than that of a larger opening area. Therefore, adjustments were made to narrow the opening area at the smaller opening (or shallower part of the mirror) and extend the opening area at the larger opening (or deeper part of the mirror). To design a micromirror that focuses on a 25 μm x 25 μm infrared absorbing film from a 150 μm x 150 μm infrared sensor element, requires a paraboloidal surface micromirror with a depth of 10 μm and an index of 2.4×10^{-3}, set at a distance of 130 μm from the concentration spot of the infrared ray as shown in Figure 1.13. Figure 1.14 shows a mask drawing of a micromirror calculated from the above calculation and Figure 1.15 shows a SEM photograph of a micromirror array consisting of 16 x 16 micromirrors arranged in an array.

As shown in Figure 1.16 an ideal shape was obtained when cross-section of micromirror was compared the actual measurement with the calculate value.

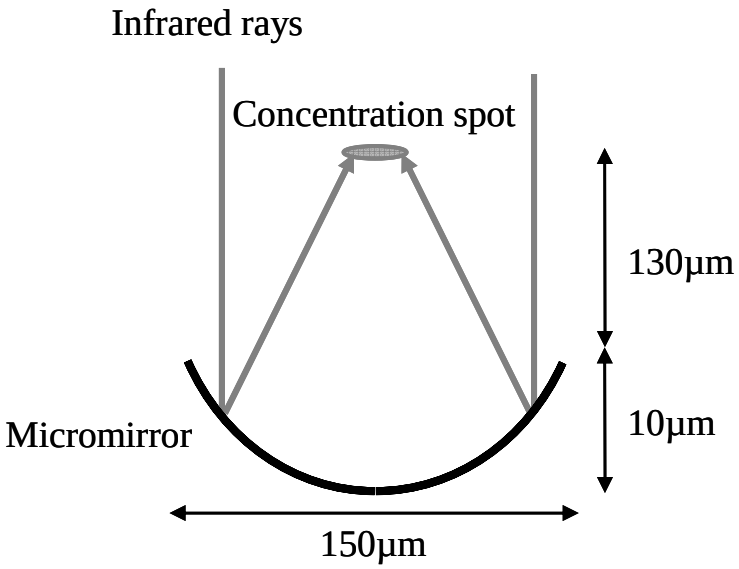


Fig.1.13 Schematic of micromirror design.

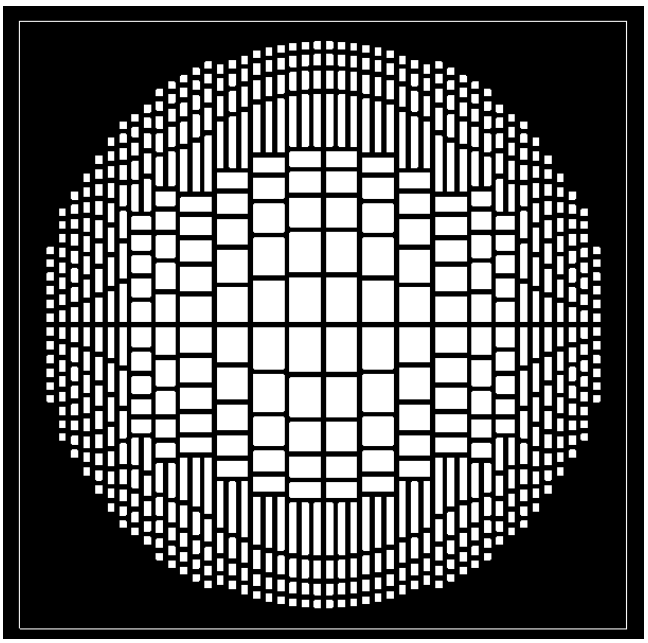


Fig.1.14 Mask drawing of micromirror.

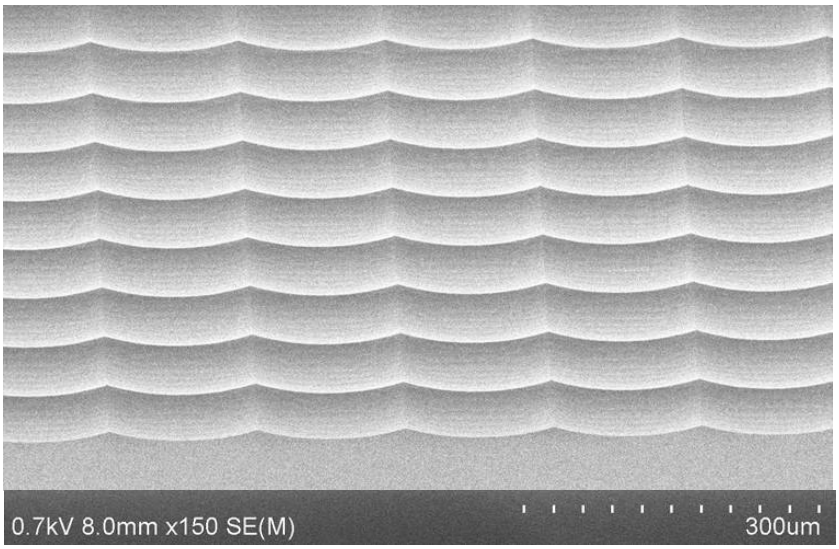


Fig.1.15 SEM photograph of micromirror array.

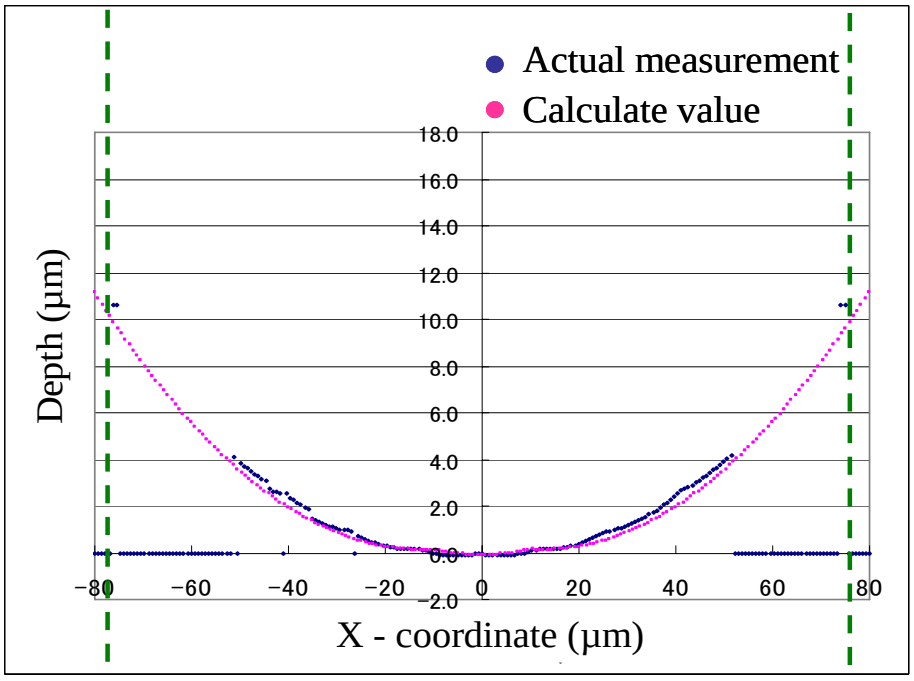
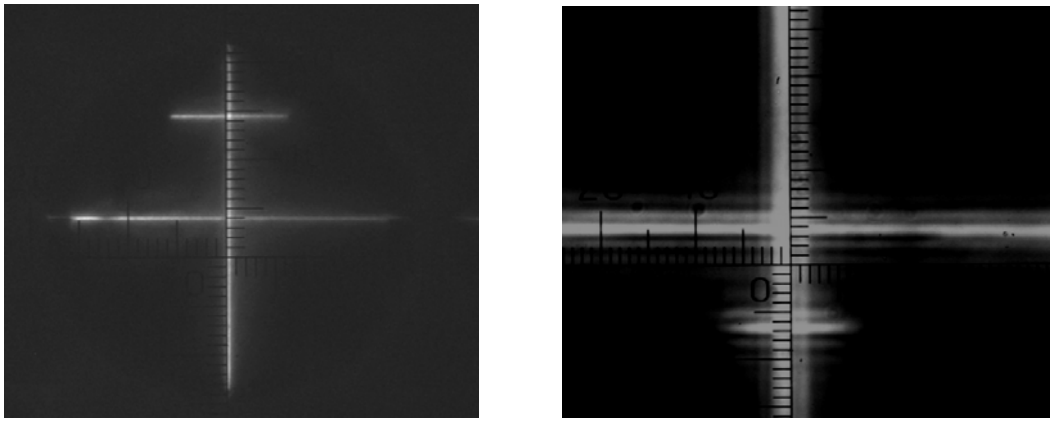


Fig.1.16 Micromirror cross-sectional shape compared actual measurement with calculate value.

1.3 Results

The focal distance was measured to evaluate the micromirror array. Figure 1.17 shows the result of a measurement conducted using a reflection type eccentricity measurement apparatus. Figure 1.17(a) shows a chart pattern image at the real image focal point and Figure 1.17(b) shows an image at a virtual focal point. By measuring the difference in focal distance between the real image and virtual image, the focal distance was 145 μm against the designed distance of 140 μm. The actual focal distance was almost as designed.



(a) Real-image photograph (b) Virtual-image photograph

Fig.1.17 Photographs taken with a reflection type eccentricity measurement apparatus.

Light intensity changes caused by differing light concentrations were evaluated by using incident-light from an optical microscope after formation of Au film on the micromirror arrays. Figure 1.18 shows an optical microscope photograph taken with incident-light illumination and focusing on

the flat surface, with a magnification of 20 and set at the minimum aperture.

On reading the light intensities at the flat surface and the concentration area by the micromirror, 10-time stronger light intensity than that at the flat place was confirmed at the concentration area after adjustment by the charge coupled device (CCD) sensitivity curve. Based on the evaluation, the effect on sensitivity improvement upon incorporation of the micromirrors to the sensor was calculated by using a ray-trace simulation. Figure 1.19 shows the ray-trace simulation model used. As shown in Figure 1.19, upon parallel light emission from the top of the infrared sensor, a 5-time stronger light intensity was proved to have entered the infrared absorbing film at the concentrated place than at the flat place, from the result of the ray trace simulation after taking into account the surface scattering factor based on concentrated light intensity on the micromirror surface. This figure seems to indicate, as expected, that the light concentration ratio of 10-time was halved due to transmission loss of infrared rays into the Si substrate of the infrared sensor.

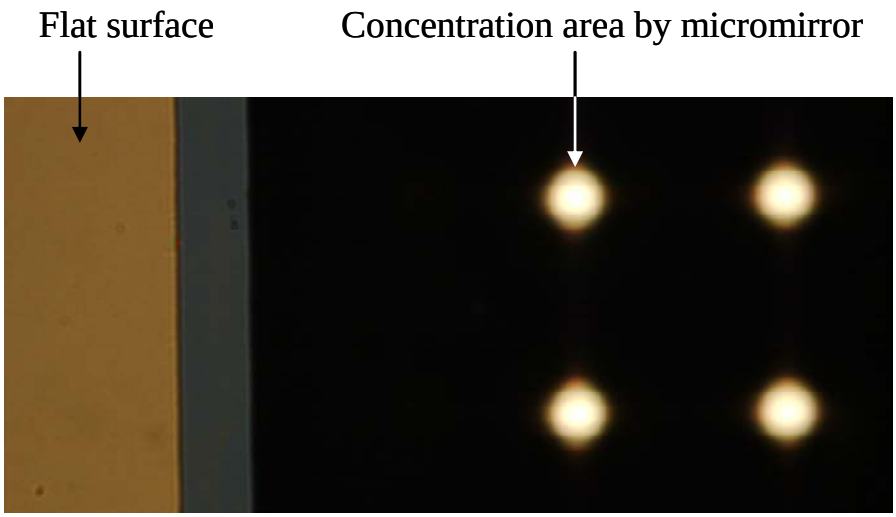


Fig.1.18 Optical microscope photograph of micromirror with incident-light illumination and focusing on the flat surface.

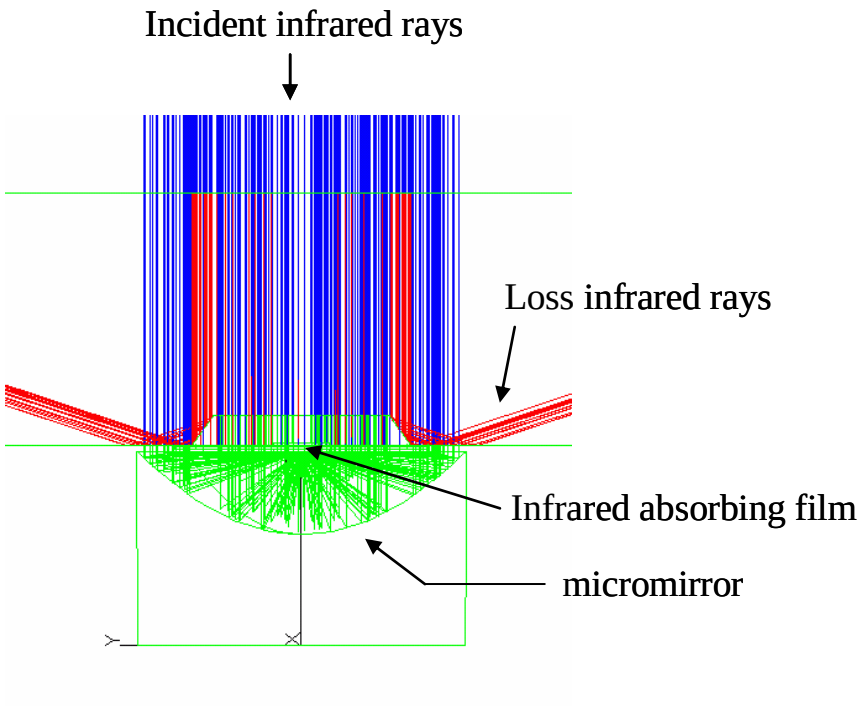


Fig.1.19 Ray-trace simulation shown in a cross-sectional view.

In the next step, the effect of infrared ray concentration was examined after setting the infrared sensor array and the micromirror array face-to-face. After attaching the infrared sensor array and micromirror array chip-to-chip with metal-to-metal bonding, they were mounted on a TO-8 size metal stem. Figure 1.20 shows a cross-sectional views of infrared MEMS array sensor.

A blackbody furnace was placed facing the metal stems and infrared rays were emitted to compare the output voltage with and without micromirrors. From the comparison, a 1.3-time higher output voltage with the mirror array than without the mirror array was proved.

The difference between the actual output voltage and the simulated 5-time higher output voltage seems to be caused by the reduction of the amount of infrared ray to 30% of the original expectation, which was a result of (i) larger light-shielding due to the increased bridge width at the time of test model creation and (ii) a reduced (100) bottom plane area constituting the infrared ray opening window.

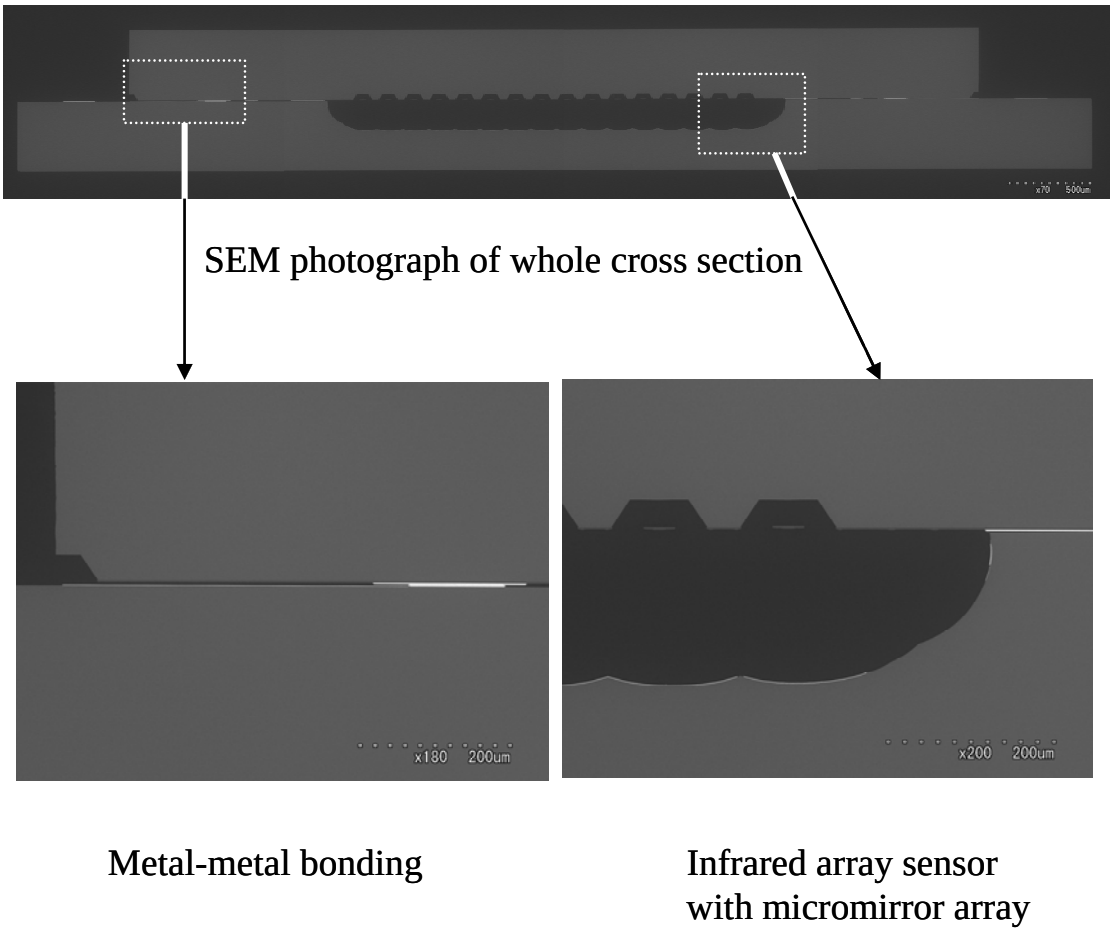


Fig.1.20 Cross-sectional views of infrared MEMS array sensor.

As it was adopted that a test model processing rule of poly-Si line width at 6 μm, the space at 4 μm and distance between the ends of the thin film at 4 μm, the bridge width becomes 24 μm, and the (100)-plane area becomes narrower due to the longer etching time of the substrate under the bridge. If the new test model can be adopt a processing rule of poly-Si line width at 1.5 μm, the space at 1.5 μm and the distance between the ends of the thin film at 3 μm, which experienced during the MOS process, the bridge width will become 10.5 μm, the (100)-plane area will become 2.5-time larger than the test model, light-shielding by the bridge will be decreased to 80% of the test

model, and the new test model consequently will be able to gain about a 4-time higher output voltage, which is almost as simulated.

In addition, when the metal stems were placed in a container, in a depressurized to vacuum state they were proved to have a 1.4-time higher output voltage than that of sensors placed on stems in an atmospheric state. The thin film which influences most to the output of the infrared sensor is made of poly-Si which has a 100-time higher thermal conductivity than that of an insulation film such as silicon dioxide film or silicon nitride film. As stated above, if the poly-Si line width becomes 1/4 times the test model from 6 μm to 1.5 μm, the total thermal conductivity will become 28% of the test model, the temperature at the hot junction will be increased in proportion to the decreased total thermal conductivity, and the new test model will be able to gain about a 7-time higher output voltage.

1.4 Discussion

When such high-sensitive infrared MEMS 16 x 16 array sensor is mounted on a package, horizontal interconnection-types are commonly adopted such as the monolithic type which mount MEMS sensors on the same substrate as the IC, or the side-by-side mounting type of IC and MEMS sensors after making them on different substrates.

The monolithic type is advantageous in that IC and MEMS are integrated, whereas its chip size tends to be large because the chip includes both IC and MEMS. In addition, the high yield of IC could be canceled out by the low yield of MEMS. This may lead to cost increase. In addition, the monolithic type has a disadvantage that MEMS processes may be limited if IC process affinity is secured.

The side-by-side mounting type might increase the yield and allow MEMS-specific processes. However, this type requires extra space such as

for wire bonding to connect IC and MEMS in the height direction and for the footprint, and this imposes a limit on miniaturization. In addition, this type has a disadvantage as it requires mounting of individual elements separately and therefore, batch processing is not applicable.

Both monolithic and side-by-side mounting types require a large footprint and, as MEMS is a structure exposed to atmosphere, a hermetic package is required to improve the heat insulation properties through reduction of internal pressure, which increase volume and production cost. In addition, it is necessary to consider the decrease in the hermetic level with the out gases generated from constitution materials [10].

To solve the above issues, it is necessary to develop the technology that can integrate infrared MEMS array sensor and IC in the vertical direction. This structure will enable manufacturers to apply optimum processes for both MEMS and IC as they are processed on different wafers, and to take advantage of the effect of optimum cost reduction by batch processing in semiconductor production as they are mounted at the wafer level.

In addition, since IC is structured to protect MEMS, no protection package is, in general, required. And further, minimum-volume terminals can be produced as the total thickness of the sensor is the thickness of post-polished IC and MEMS substrates with no requirement for wire bonding, etc., and, minimization of the footprint can be achieved due to vertical piling of MEMS and IC.

To realize this structure, the interconnection that electrically connects IC to MEMS in the vertical direction will become the key. This technology, “MEMS-semiconductor vertical interconnection technology”, is the main theme of this thesis. This technology is to form fine and high-aspect ratio through-holes, to form high-aspect ratio through-hole interconnection, and to realize wafer-level mounting by damage-less low temperature bonding technology and wafer-level packaging technology. The low temperature bonding technology and wafer-level packaging technology can keep a vacuum

inside of infrared MEMS array sensor in itself to bond micromirrors to infrared sensors directly and realize in particular the high-sensitive infrared MEMS array sensor without a hermetic package.

Details of the technology will be described in Chapter 2 and subsequent chapters.

1.5 Conclusion

Concerning high-sensitive infrared MEMS array sensor, this chapter has proposed the following: (a) a method that sets micromirrors one to one for each sensor to concentrate infrared rays in order to increase the sensitivity of the thermopile sensor method which is suitable for semiconductor processes and (b) a structure that enables individual chips to realize increased heat insulation and increased hot junction temperature and have verified the results on infrared sensors and micromirrors.

The infrared MEMS array sensor consists of 16 x 16 sensors of 150 μm x 150 μm each. A thermopile connecting p-type Si interconnection and n-type Si interconnection on the insulation membrane created by anisotropic wet etching on the surface of the Si wafer is used as a temperature sensor. Micromirrors are fabricated by making holes with different depths on the Si substrate using the lag effect of DRIE, smoothing the side walls by isotropic etching and forming a reflective surface by vacuum deposition of Au on the surface. The required design and process parameters were extracted from experimentation of the relationship between the opening area and etching depth. As designed, the intersectional shape and a focal distance of 145 μm were obtained.

The infrared array sensor and micromirror array were bonded face-to-face at chip level and mounted on a TO-8 size metal stem and the effect of infrared ray sensitivity was measured upon exposure to a blackbody furnace. A

1.3-time concentration effect by the mirror and a 1.4-time thermal insulation effect under vacuum conditions were obtained. In addition it was found that a 4-time larger concentration effect, a 7-time larger vacuum's thermal insulation effect and, nearly a 30-time more sensitive infrared sensor in total than the test model by narrowing the width of poly-Si interconnection line of the thermopile from 6 μm to 1.5 μm are obtained.

The necessity of through-hole interconnection and wafer level bonding required to realize small and low-cost high sensitive infrared MEMS array sensor has been described.

References

[1] T.Taniguchi, R.Sato, and M.Ohba, IEICE Technical Report, Vol.83, No.237, **7**, 1984

[2] M.Sakata, K.Hosoya, and M.Ohba, J. Robotics and Mechatronics, Vol.3, No.1, **47**, 1991

[3] R.A.Wood, C.J.Han, and P.W.Kruse, Tech. Digest of IEEE Solid-State Sensor and Actuator Workshop, **132**, 1992

[4] Y.Kosasayama, T.Sugano, Y.Nakaki, Y.Fujii, H.Inoue, H.Yagi, H.Hara, M.Ueno, M.Takeda, and M.Kimata, Proc. SPIE, Vol.5406, **504**, 2004

[5] H.Hirota, Y.Ohta, and Y.Fukuyama, Proc. SPIE, Vol.6940, **694032-1**, 2008

[6] Y.Ohta, Y.Arakawa, T.Fukumoto, Y.Fukuyama, and M.Hirata, Proc. the 26th Symposium on Sensors, Micromachines & Applied Systems, **622**, 2009

[7] T.Ishikawa, M.Ueno, K.Endo, Y.Ohta, J.Nakanishi, K.Kasasayama, H.Yagi, T.Sone, and M.Kimata, Proc. SPIE, Vol.4130, **152**, 2000

[8] T.Ohori, T.Takahata, E.Iwase, K.Matsumoto, and I.Shimoyama, Proc. the 24th Symposium on Sensors, Micromachines & Applied Systems, **15**,

2007

[9] M.Ohira, Y.Koyama, F.Aita, S.Sasaki, M.Oba, T.Takahata, I.Shimoyama and M.Kimata, Proc. the 26th Symposium on Sensors, Micromachines & Applied Systems, **328**, 2009

[10] M.Ohba, K.Kuzukawa, and K.Ozawa, Components, Hybrids, and Manufacturing Technology, IEEE Trans. Vol.11, Issue 1, **85**, 1988

Chapter 2

Design and fabrication of high-aspect ratio dry etching and insulator deposition

2.1 Introduction

Vertical interconnection methods are attracting attention as technology that satisfies miniaturization and high integration requirements for electronic devices. However, existing generally available vertical interconnection methods are mainly employed in relatively large items such as printed circuit boards and ceramic boards [1]. Vertical interconnection methods as used for MEMS technology started with devices built by forming through-holes in a glass wafer and applying electric interconnection materials to the side walls of the holes by vapor deposition or sputtering [2], and have evolved to include techniques for forming through-holes in a silicon wafer and filling the holes with molten metal as electric interconnections [3]. In the meantime, through-hole formation technology, which advanced as part of MEMS technology, is at present, starting to be actively deployed in the LSI technology field [4-5]. As wafers can be very thinly polished to form devices in LSI, through-holes with comparatively low aspect ratios are sustainable for practical use.

In contrast, since MEMS devices are of a three-dimensional structure, not only is there difficulty in producing thin wafers by using polishing or other such methods, but as a consequence of using existing hole formation technology, through-holes occupy a large surface area within the device due to their large minimum diameters and low aspect ratios, resulting in few practical examples of using vertical interconnection methods within MEMS devices.

According to Table 2.1, when applying a dry etching method with DRIE equipment, the maximum through-hole aspect ratio is about 12 at present.

Even with the use of photo assisted electro chemical etching (PAECE) method, which is able to achieve a higher aspect ration through use of selected silicon crystal orientation, the aspect ratio is only 35 [3].

Table 2.1 Comparison of through-hole formation methods.

	Dry etching	Wet etching	Laser ablation
Process method	DRIE	PEACE	Laser-drilling
Hole diameter < 5 μm	△ 10 μm	△ 15 μm	× 60μm
AR > 50	○ ～50	△ 35	△ 10
Material Processed	○ Si, Glass, GaAs, etc.	△ n-type Si	○ Si, Glass, GaAs, etc.
Wafer surface roughness	× Metal, SiO_2	○ Resist	○ Mask-less
Process time	△ 1μm/min	△ 1μm/min	× 1sec/via (processing time only)
Hole shape	○ Scallop, taper(small)	× With side branch	× Taper(large)

To form high-aspect-ratio through-holes, reactive ion etching (RIE) technology is often selected because it is a reactive ion etching method that is more highly anisotropic than other dry etching methods. Ion etching is a process technology that uses ions generated by plasma discharge in a low-vacuum environment. The RIE is an ion etching technology that uses a

reactant gas when etching the silicon substrate, in order to enhance the processing performance. The constituents of plasma are ions, which are either in the state of a reactive gas or in the state of non-molecular bonded radicals. Since radicals are chemically unstable, they are highly reactive and work as an isotropic etching agent with an extremely high etching rate.

In order to increase the etching rate, the inductively coupled plasma (ICP) etching method is often used, which generates strong plasma enclosed in an electromagnetic field produced by a high-frequency inductor installed to surround the etching apparatus.

Similar to infrared MEMS array sensor, MEMS devices are often structured from silicon substrates where it is not rare for the depth of a through-hole to exceed 300 μm. In RIE and ICP methods where the maximum hole diameter to hole depth ratio is about 5, the hole diameter will increase in proportion to the hole depth, resulting in the need for considerably larger chip areas.

To deal with this difficulty, the Bosch Process, which alternately repeats two modes of silicon etching and side walls protection, was developed by F.Larmer and A.Shilp at Robert Bosch GmbH in 1992.

Figure 2.1 shows Bosch process overview. Firstly, the silicon undergoes isotropic etching with an SF_6 radical gas resulting in a round hole being formed on the resist and then on the silicon substrate. Next, a C_4F_8 gas (a type of chlorofluorocarbon) is introduced, which reacts with the plasma to produce a fluorocarbon polymer, which sticks to the side walls and bottom of the hole in a film. When the gas is changed to SF_6 again, only the polymer at the bottom of the hole is etched by the electric field produced as the SF_6 ions expose the bottom of the silicon substrate. Isotropic etching proceeds to form a round etched area on the bottom of the hole from the chemical reaction between the silicon substrate and SF_6 radicals. When these steps are repeated at intervals of several seconds, a deep vertical hole with high-aspect ratio is formed.

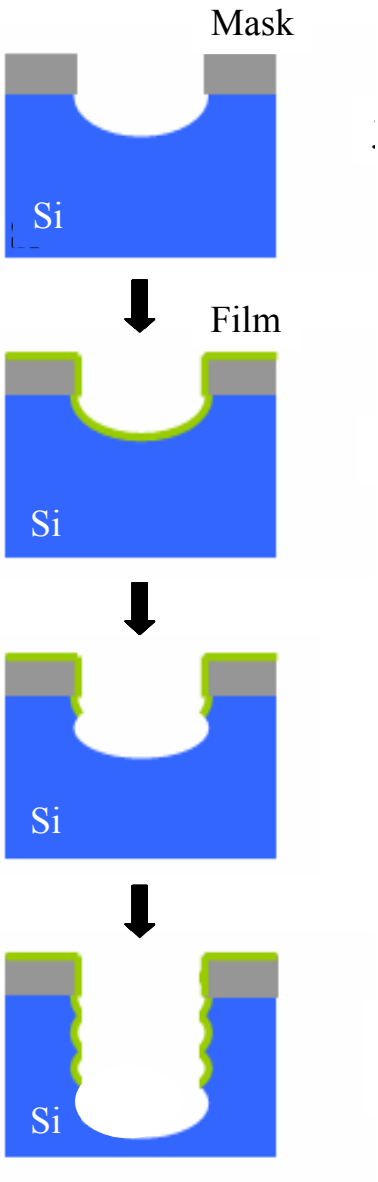


Fig.2.1 Schematic illustrations of Bosch process.

The only existing method in reproducing high aspect ratio processing was the LIGA (LIthograpie Galvanoforming, Abformung in German) method which uses hard X-rays from synchrotron radiation. The Bosch Process is a very important technology in that it can reproduce high aspect ratio processing

inexpensively and is not limited only to through-hole formation but can also be utilized to form deep-groove structures such as comb electrodes for accelerometers and gyroscopes.

When LSI and MEMS are bonded to form a multilayer structure, the vertical interconnections are required to penetrate completely through both the LSI and MEMS wafers. When forming electrode pads based on the 65-nm rule that LSI is assumed to fulfill in the future, the inter-pad pitch is thought to become about 10 μm. Taking into account the process allowance required to form through-holes in the thick MEMS wafers (typical thickness of about 250 to 500 μm) compared with that of thin LSI wafers, holes with diameters of up to 5 μm diameter and an aspect ratio of at least 50 will be required.

In actual fact, the required pitch of 10 μm for face-to-face interconnections matches the data found in LSI's standard roadmap index, The International Technology Roadmap for Semiconductors (ITRS) 2005 edition, concerning the System in Package (SiP) process in Table 100 on page 36 of "Assembly and Packaging".

On the other hand, as the wafer thickness is restricted to less than 20 μm, according to the table concerning inter-LSI SiP, the aspect ratio is about 4. If the diameter of the through-holes in MEMS device wafers is assumed to be about 5 μm, aspect ratios of higher than 50 are required to ensure that the resulting MEMS devices can be put into practical use. Therefore, special development efforts are required in this field.

2.2 High-aspect ratio dry etching

A hole structure with a 5 μm diameter and a 50:1 aspect ratio has never been formed by a dry etching method yet. In order to realize a dry etching technology of high-aspect ratio products, not only the performance of dry etching equipment but the following technologies are required.

-Thick film resist technology with the thickness determined by the etching rate ratio.
-A deep-drill etching technology that forms through-hole side walls in desired shapes.

Details about these technologies are described in the following section:

2.2.1 Experimental procedure of thick film resist for dry etching mask

The resist mask was developed for a dry etching mask. As metal masks and oxidized film masks are known for their adverse influences on surface roughness after the formation and removal of the masks, considering process affinity, the mask development was based on the concept of using resists that are easily formed and removed with little damage to the wafer surface. However, to form high-aspect-ratio through-holes, thicker films are required to ensure the use of resist masks with a higher etching rate than in the case of using metal masks or oxide masks.

An etching rate becomes small and the etching selectivity of resist on the surface of a Si wafer becomes small relatively, so that the hole diameter which etching by DRIE is formed in a Si wafer becomes small, and, so that the depth of a hole becomes deep. In the case of through-hole with a 10-μm diameter, depth of 400 μm, and through-hole with a 5-μm diameter, depth of 250 μm, the resist thickness of at least 15 μm is necessary, even if the etching selectivity in a shallow portion is around 40, since the etching selectivity in a deep portion becomes small with around 10, it is synthetically needed the etching selectivity of 25. Consequentially, the resist thickness was determined as total 30-μm thick in consideration of the wafer surface protection and deviation of processing.

In addition, the shape of the resist mask, especially the diameter of the

mask hole through which the wafer is exposed, is primarily determined by the wafer thickness under a given exposure condition. Therefore, uniform resist film thickness distribution is required to ensure that the resist mask shape does not vary at different locations on the wafer. The standard deviation (SD) of the thickness of thick film resists (30 μm) obtained when only the speed of wafer rotation was controlled at the time of resist coating was SD of 1.01, which is equivalent to a 1.5 μm deviation of mask hole diameter.

A resist film thickness in forming thick films of less deviation, SD of 0.41 was achieved due to measures such as the introduction of a resist suitable for thick films, resist viscosity adjustment based on temperature control, the application of a vacuum baking process, and the optimization of the exposure wavelength, in addition to the control of wafer rotation speed at the time of coating as mentioned above.

Process conditions were thus obtained to reduce the mask hole diameter deviation to 0.3 μm. More specifically, a pre-cooled resist (PMER P-VS 1000PM manufactured by Tokyo Ohka Kogyo Co., Ltd) with a viscosity of 1 Pa･s (1000 cP) was applied to wafers using a coater and the wafers were placed in a vacuum oven where they were deaerated at room temperature for smoothing. Figure 2.2 shows the resist film thickness distribution. As a result, the variance σ of the film thickness distribution over the wafer surface was improved to 0.3 μm from 1.4 μm when compared with the condition in which wafers were left at room temperature for 20 minutes. For film thickness measurement, a micro-spot spectroscopic reflectometry (NanoSpec manufactured by Nanometrics Inc.) was used at 17 points arranged in a cross over the wafer surface.

The wafer was pre-baked in an N_2 atmosphere for exposure and development. The cross-sectional view and results of film thickness measurement of a test-fabricated resist mask are shown in Figure 2.3 and Table 2.2 respectively.

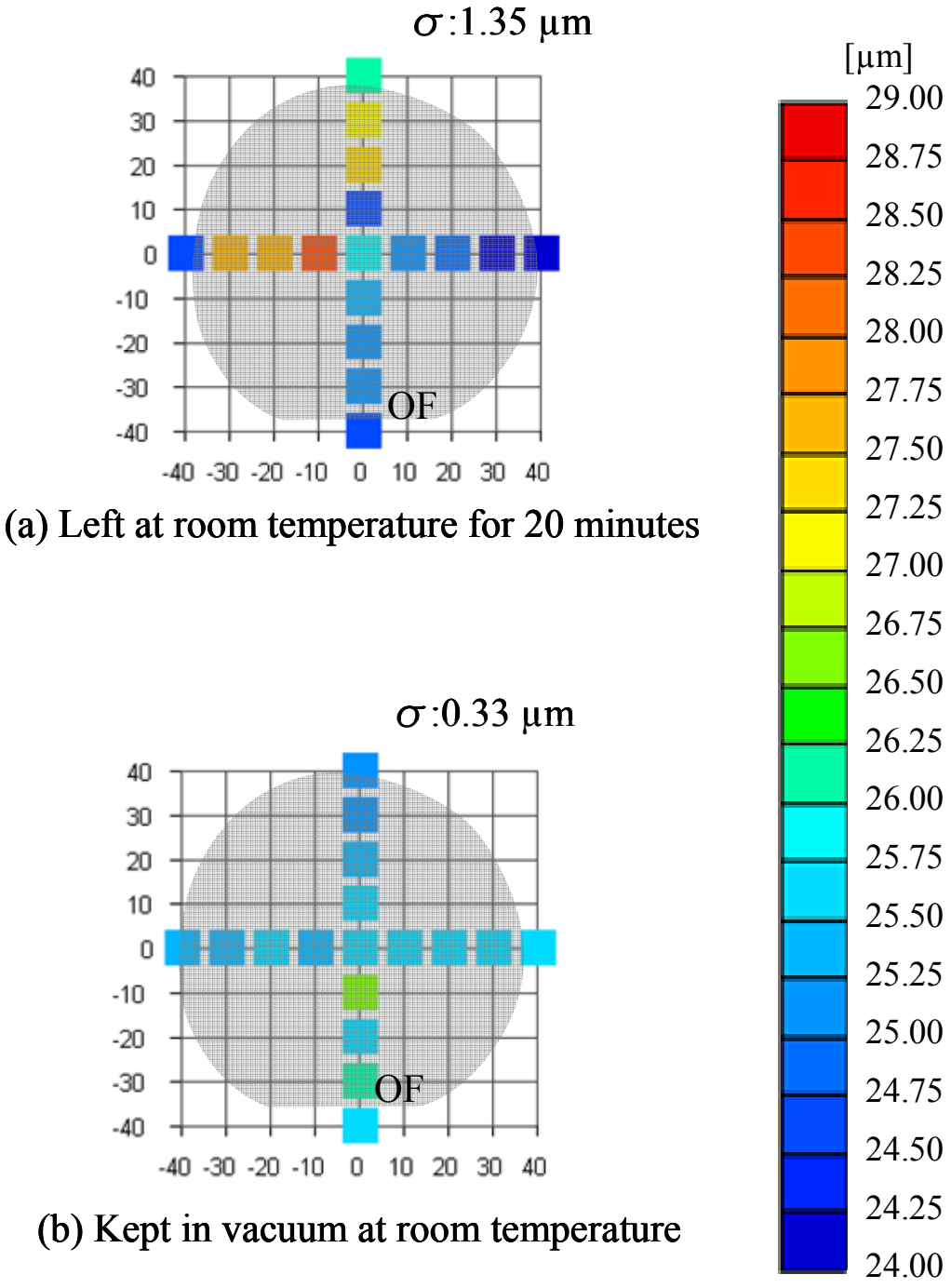


Fig.2.2 Resist film thickness distribution over the wafer surface.

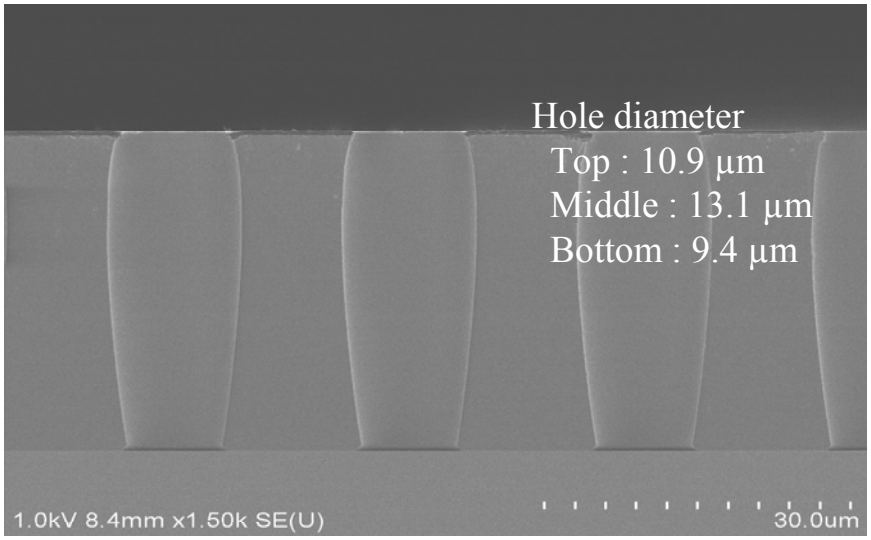


Fig.2.3 Cross-sectional view of thick film resist mask.

Table 2.2 Thick-film resist thickness measurements.

x(mm)	Film thickness (μm)
-40	30.82
-30	30.29
-20	31.42
-10	31.22
0	31.35
10	30.43
20	30.82
30	30.56
40	30.56

x(mm)	Film thickness (μm)
Ave.	30.83
Max.	31.42
Min.	30.29
SD	0.41

2.2.2 Experimental procedure of high-aspect ratio dry etching

It is difficult to judge the feasibility of a particular high-aspect dry etching technology based on the specifications of the equipment and past records. Therefore, formation of actual through-hole structures was tested by using five generally available DRIE etching equipments and was assessed the results.

Comparative evaluation were conducted by the test models with importance placed on the shape of the side-walls of the through-holes, which are a significant indicator of the ability of each model in forming high-aspect-ratio structures for improving the aspect ratio. Figure 2.4 shows the result.

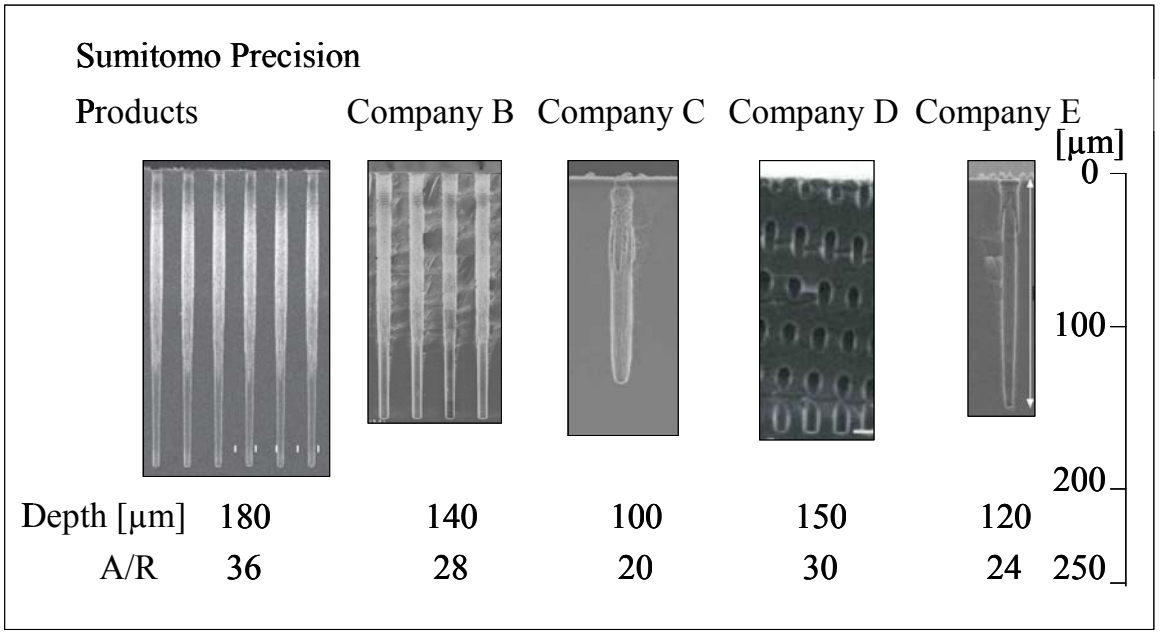


Fig.2.4 Through-hole formation test using 5 main companies' DRIE equipments.

Based on the result of the comparative test, the ASE-Pegasus (Figure 2.5) dry etching equipment manufactured by Sumitomo Precision Products Co.

Ltd. was selected, because it produced the flattest side walls and the deepest, high-aspect ratio holes. The high-aspect ratio dry etching technology was constructed by using this equipment.

Fig.2.5 Photograph of DRIE equipment (ASE-Pegasus).

For this, extraction of etching conditions that will achieve a high selection ratio to the resist is asked for. Unfortunately, high-aspect ratio etching that will produce through-holes with an aspect ratio of higher than 50 is likely to fail during the process of smooth gas switching and is unlikely to achieve smooth etching and the gas desorption reaction without difficulty. In order to increase the etching rate in this environment, it is necessary to depend on ion

reactions and set a rather high bias output, but this will tend to decrease the selection ratio to the resist.

The problem to be solved here is the unstable side-wall shape. The active species contributing to etching are radicals that are not electric-field dependent, unlike those that are ions. As such radicals (active species) disturb the straightness of through-holes being produced by high-aspect-ratio etching, it is necessary to control the protective film thickness at the depth reached by the radicals, depending on the etching depth. Considering the above, high-aspect ratio etching was developed based on the concept that by setting meticulous conditions at various etching depths, and it was obtained that etching conditions can be flexibly adapted to the set etching depth conditions.

2.2.3 Results and Discussion

As indicated in Table 2.3, by precisely controlling the optimum etching conditions of the gas-plasma follow-on process, depending on the optimum etching depth and area, as shown in Figure 2.6, for an Si wafer of thickness 525 μm, vertical holes of 10-μm diameter and a 50:1 aspect ratio were formed. This pre-verified that the technique used will be useful for through-hole formation.

The hole diameter is 10 μm at the bottom, in contrast to the larger 17 μm diameter in the middle. Although it is a barrel-shaped vertical hole, when used for as a signal interconnection, will have high reliability from the strong interconnection securing force due to the adhesion between the interconnection and the vertical hole side wall. For example, when the lead-free solder reflow process reaches as high as 250°C, the barrel-like shape will work as a stopper when the metal in the through-hole expands as the metal has a higher linear expansion coefficient than the Si substrate.

Table 2.3 DRIE conditions for forming holes with a 10-μm diameter and a 50:1 aspect ratio.

Step	Gas species	Flow rate (sccm)	Step time (sec.)	Pressure (Pa)	Coil Power (W)	Platen Power(W)
1	C_4F_8	400=>480	2.0=>2.3	6.0=>7.6	2000=>2400	0
2	SF_6	350	0.2	2.0	2000	30=>90
3	SF_6	350	1.8	2.0	2000	30=>90
4	SF_6	300	1.1=>1.8	8.0	2000	5

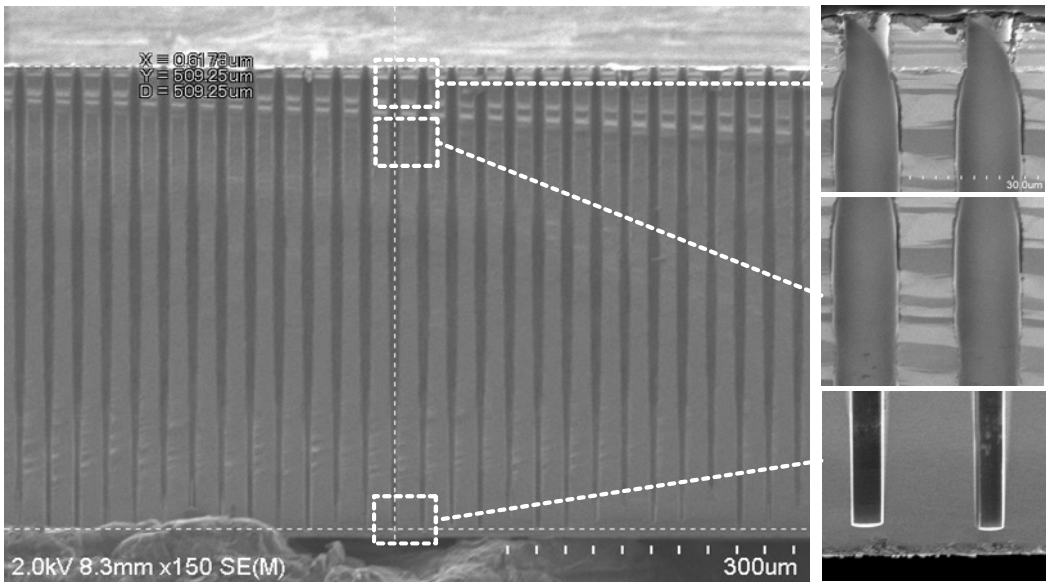


Fig.2.6 Cross-sectional views of micro holes with a 10-μm diameter and a 50:1 aspect ratio. (wafer thickness: 525 μm)

As a next stage, process conditions for the formation of 5-μm diameter holes into a 400-μm-thick Si wafer were developed, and it was confirmed that an etching depth of 273 μm was achieved in these conditions.

Table 2.4 shows DRIE conditions and Figure 2.7 shows a cross-sectional view of micro holes.

Table 2.4 DRIE conditions for forming holes with a 5-μm diameter and a 50:1 aspect ratio.

Step	Gas species	Flow rate (sccm)	Step time (sec.)	Pressure (Pa)	Coil Power (W)	Platen Power (W)
1	C_4F_8	400=>489	2.0=>2.6	6.0=>9.2	2000=>2444	0
2	SF_6	350	0.2	2.0	2000	30=>90
3	SF_6	350	1.8	2.0	2000	30=>90
4	SF_6	300	1.1=>2.5	8.0	2000	5

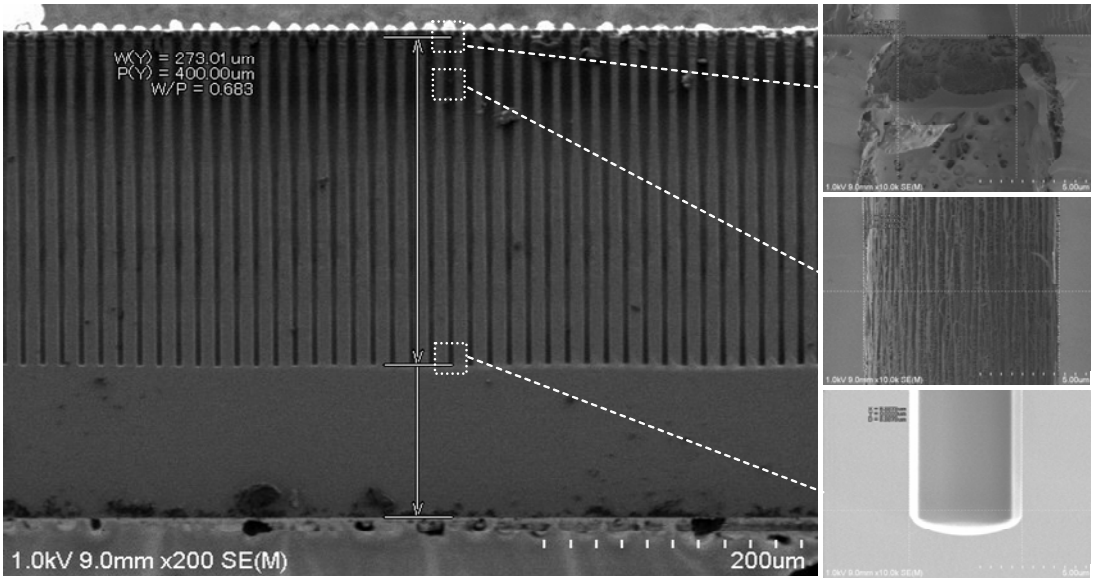


Fig.2.7 Cross-sectional views of micro holes with a 5-μm diameter and 273-μm depth. (wafer thickness: 400 μm)

Vertical micro holes were compared the nominal 5-μm diameter with 10-μm diameter at the top, middle and bottom (Table 2.5). All holes with either nominal diameter were of the above barrel structure. That is to say, the diameter at the middle was greater than that at surface of the wafer. The larger diameter at the middle seems to be caused by the influence of remaining angled ionic etching and radical etching components at the middle.

Table 2.5 Actual measurement comparison of 5-μm and 10-μm micro-holes diameter.

	Micro-hole diameter	
	5-μm diameter	10-μm diameter
Hole diameter at top [μm]	5.62	9.41
Hole diameter at middle [μm]	9.25	17.03
Hole diameter at bottom [μm]	5.39	7.19

Considering based on the above result, through-hale formation conditions were studied for an Si wafer of thickness of 250 μm, vertical holes of 5-μm diameter and a 50:1 aspect ratio were formed. Figure 2.8 shows a cross-sectional view of through-hole interconnections with a 5-μm diameter formed in a 250-μm-thick wafer under the DRIE conditions indicated in Table 2.6.

This barrel-like hole, when used for a signal interconnection, seems to provide a reliable structure because of a strong interconnection securing force due to the adhesion between the interconnection and the inside wall of the through-hole.

Table 2.6 DRIE conditions for forming through-holes with a 5-μm diameter and a 50:1 aspect ratio.

Step	Gas species	Flow rate (sccm)	Step time (sec.)	Pressure (Pa)	Coil Power (W)	Platen Power (W)
1	C_4F_8	400=>500	2.0=>2.5	6.0=>8.4	2000=>2500	0
2	SF_6	350	0.2	2.0	2000	30=>90
3	SF_6	350	1.8	2.0	2000	30=>90
4	SF_6	300	1.1=>2.3	8.0	2000	5

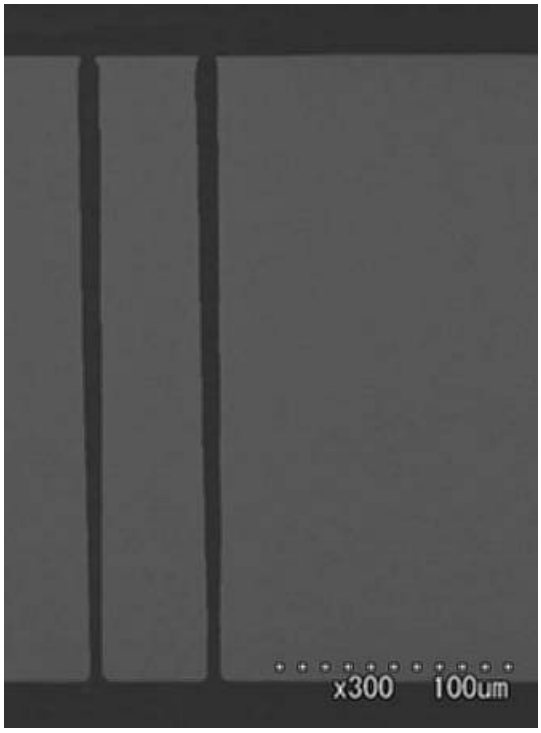


Fig.2.8 Cross-sectional view of micro through-holes with a 5-μm diameter and a 50:1 aspect ratio.
(wafer thickness: 250 μm)

Each DRIE condition shown in Table 2.3, Table 2.4 and Table 2.6 returns to step 1 again when processing is sequentially given from step 1 to 4, and repeats processing. It is shown that the set value expressed by the arrow is a ramping, and the value continuously changes whenever processing from step 1 to 4 is repeated from an initial value to the final value. The pressure value in this table means the pressure in processing chamber. Coil Power is a parameter that decides the gas how to make it to plasma. Platen Power is a parameter that decides whether to draw the ion ingredient of plasma by strength of which extent.

2.3 Double-side etching on SOI wafer

Double-side etching was also developed technology that can be used to form through-holes from both sides of a wafer.

An SOI wafer is generally used to manufacture MEMS devices such as accelerometers, gyroscopes and microphones, and it becomes very important to form a through-holes in SOI wafer. Additionally, this technology was used to form through-holes in a laminated MEMS wafer as shown Figure 2.9, subjected to vertical lamination of multilayer laminated MEMS devices as shown in Figure 2.10 and to form through-holes in devices created on an SOI wafer. Conventional etching technology fails to achieve formation in the above former case because of too high an aspect ratio, whereas one-side etching will not always be efficient when used for formation in the latter case.

In addition, it is not desirable to be in a state where etching of the plate section of the apparatus directly occurs with a reactive gas while forming through-holes in the wafer. To avoid this situation, double-side etching was studied to form a through-hole, that is to say, etching the wafer substrate from both sides until a through-hole was produced.

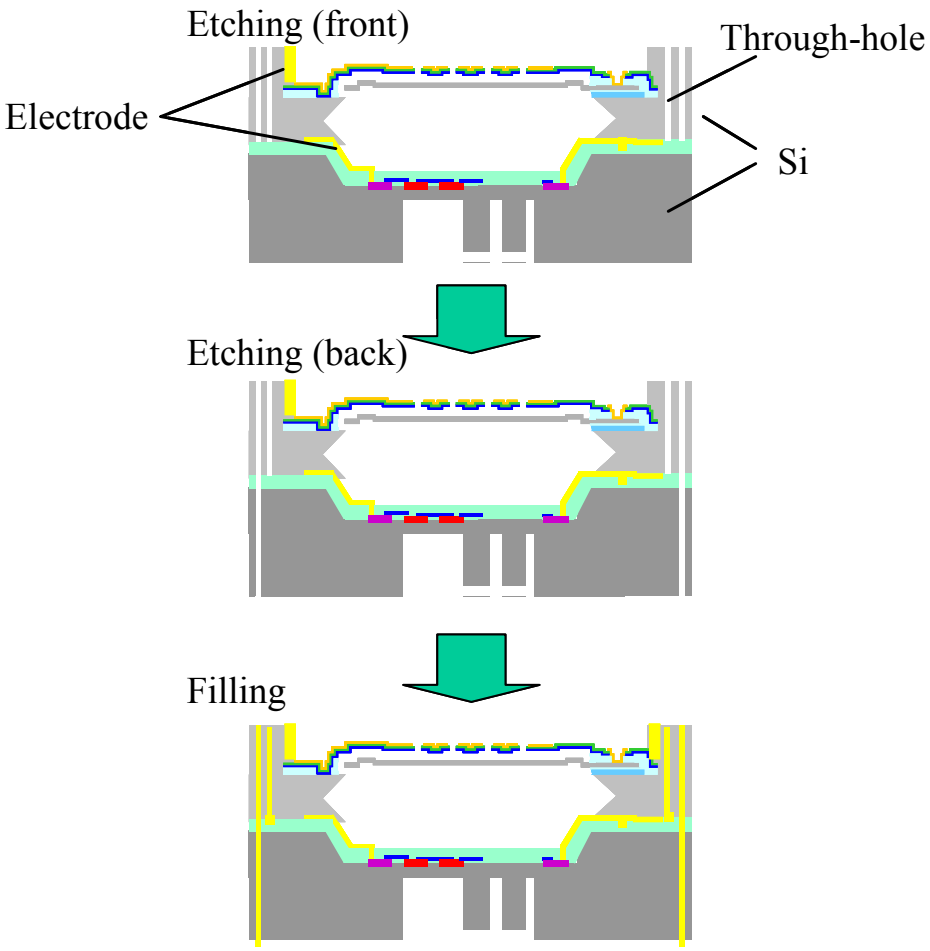


Fig.2.9 Schematic illustrations of through-hole formation process after bonding.

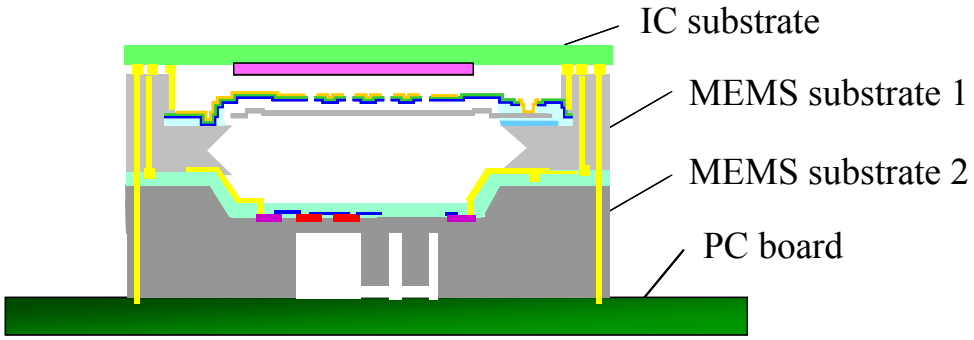


Fig.2.10 Schematic illustration of multilayer laminated MEMS device.

2.3.1 Experimental procedure

Figure 2.11 shows a cross-sectional view of DRIE etching from both sides. The figure demonstrates that through-holes with a 10-μm diameter were formed on Si wafer of 525-μm thick, with a seam being observed in the center of the wafer.

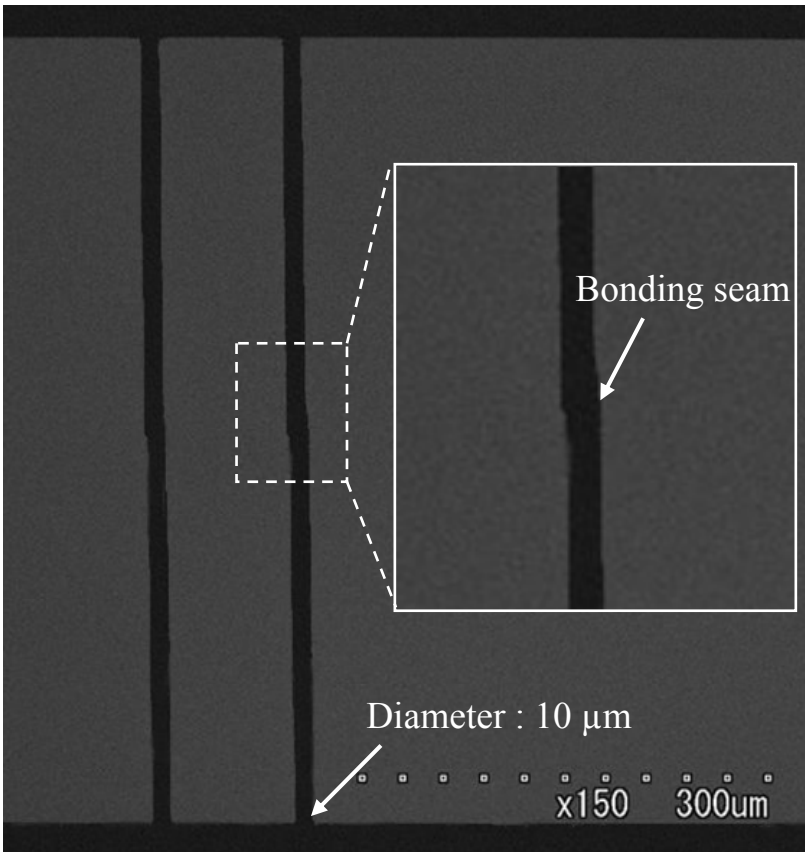


Fig.2.11 Cross-sectional views of DRIE etching from both sides.

An SOI wafer includes an oxidized film called the BOX layer between the Si active layer and the Si handle layer. Since the BOX layer works as an etching stop layer, a process that removes the BOX layer must be added. To remove the BOX layer, a wet etching process using HF solution was selected.

Because a dry etching process involves problems relating to notching and bowing during BOX layer removal and causes etching components to affect the device stage during BOX layer removal. The process was thus established the process for forming through-holes in an SOI wafer by following the flow shown in Figure 2.12.

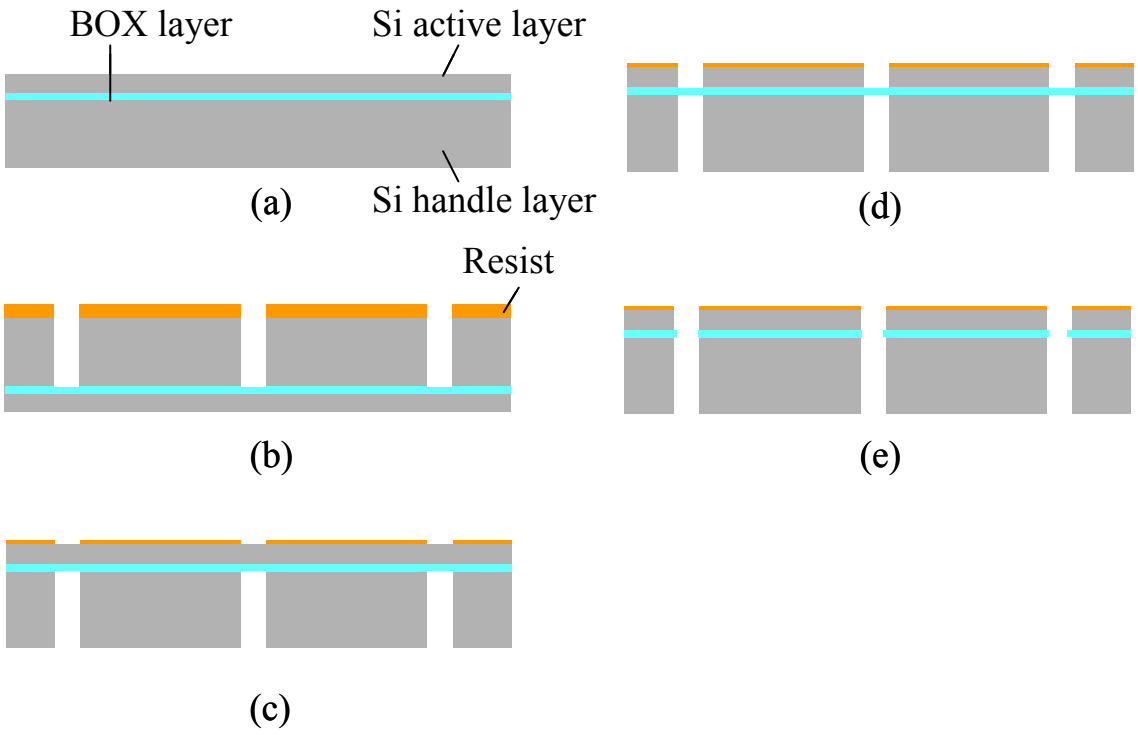


Fig.2.12 Cross-sectional schematic of SOI wafer through-hole formation process.

When etching is applied from one side to form through-holes in an SOI wafer, the holes will be shaped to bulge at the BOX layer level as shown in Figure 2.13 due to the differences in etching rate and side etching amount between the Si layers (active layer and handle layer) and the oxide (BOX) layer. It is thought from theory that this geometric singularity of the wall surface at the BOX layer level is likely to cause troubles in insulation film

formation and interconnection formation performed as part of other processes.

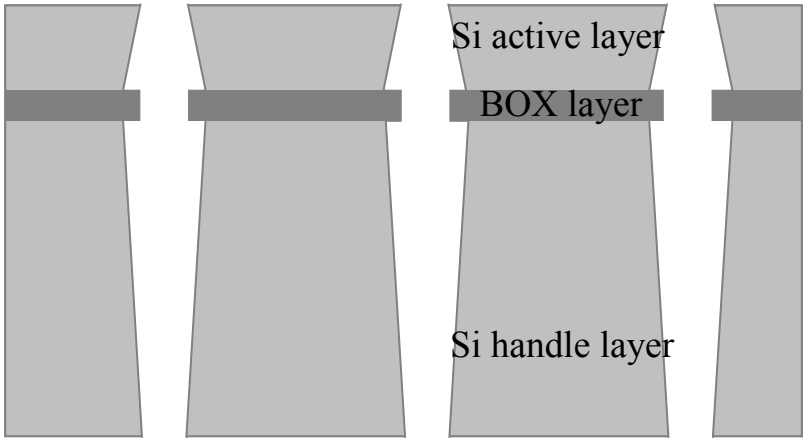


Fig.2.13 Cross-sectional patterns of an SOI wafer as etched from the above.

2.3.2 Results and Discussion

Figure 2.14 shows a cross-sectional view of a wafer where through-holes with a 10-μm diameter and 40:1 aspect ratio are formed in an SOI substrate with an active layer (10-μm-thick Si), a BOX layer (0.9-μm-thick SiO_2) and a handle layer (400-μm-thick Si). The diameter of the hole in the vicinity of the BOX layer was 10 μm, with the larger diameter of 17 μm at the bottom of the hole. In contrast to one-side etching, the lower part of the hole is a barrel-like shape but, similar to the original barrel-like hole, this shape will also be reliable when used for signal interconnection, from a strong interconnection securing force due to adhesion between the interconnection and the inside wall of the through-hole. Moreover, since the Box layer is extended in the transverse direction by HF side etching as an effect which removed the BOX layer using wet etching, it becomes shape that the electrode

also covered to extended BOX layer. It is expected that this portion serves as a role of stopper, such as the omission of the interconnection electrode at the time of polish.

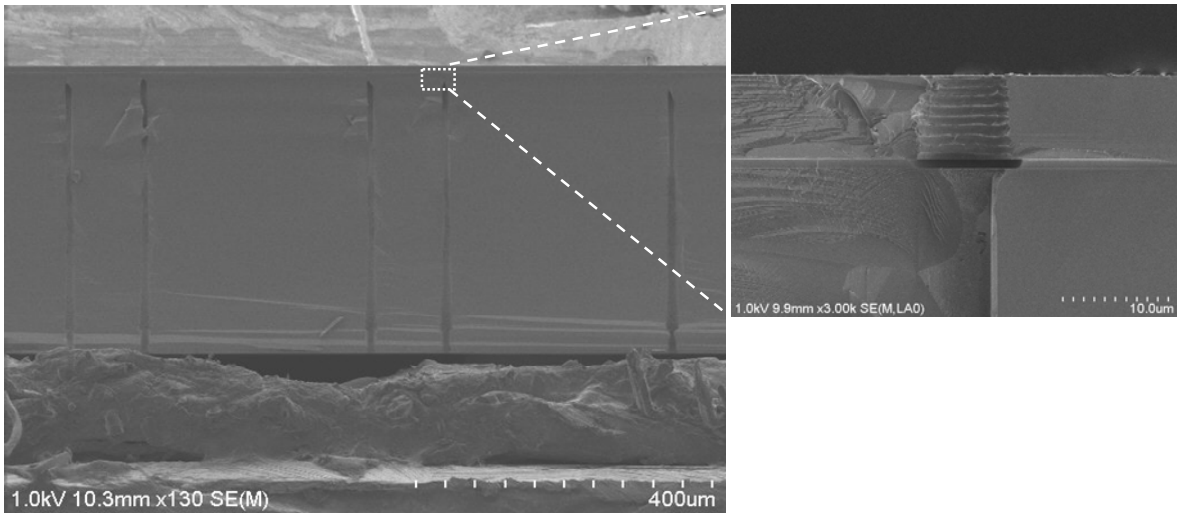


Fig.2.14 Cross-sectional views of SOI wafer through-holes with a 10-μm diameter and an aspect ratio of 40:1, formed by double-side etching.

Figure 2.15 shows a cross-sectional view of a wafer where through-holes with a 5 μm diameter and 52:1 aspect ratio are formed. The shapes of holes with a 5 μm diameter show the same tendency with those of 10 μm diameter. The diameter near the bottom of the hole is 8 μm, which is larger than that in the vicinity of the BOX layer which is 5 μm. The shape of the hole is observed to be a barrel-like shape.

Figure 2.16, which shows the central part of the wafer, demonstrates clearly the significant influence on the difference in holes position between the active layer and the handle layer on the periphery of the wafer. Therefore, an SOI wafer was conducted quantitative and causal analyses on the seam. Table 2.7 shows the result of measuring the diameters and hole-to-hole positioning accuracies of three holes in an SOI wafer.

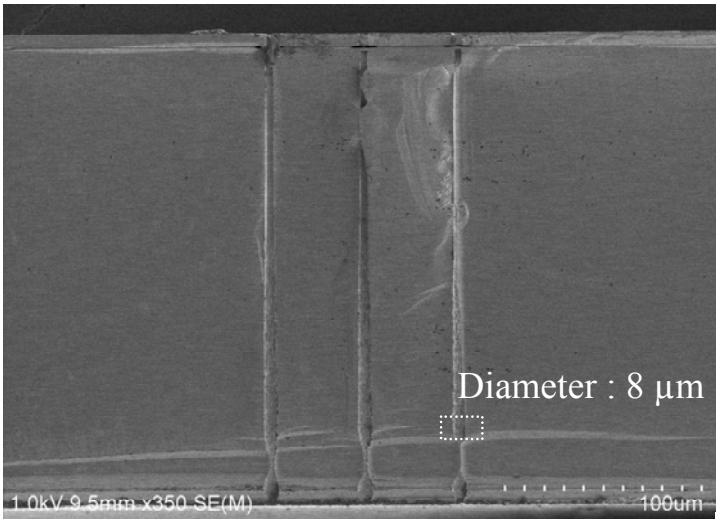


Fig.2.15 Cross-sectional view of through-holes with a 5-μm diameter and an aspect ratio of 52:1, formed through double-side etching of an SOI wafer.

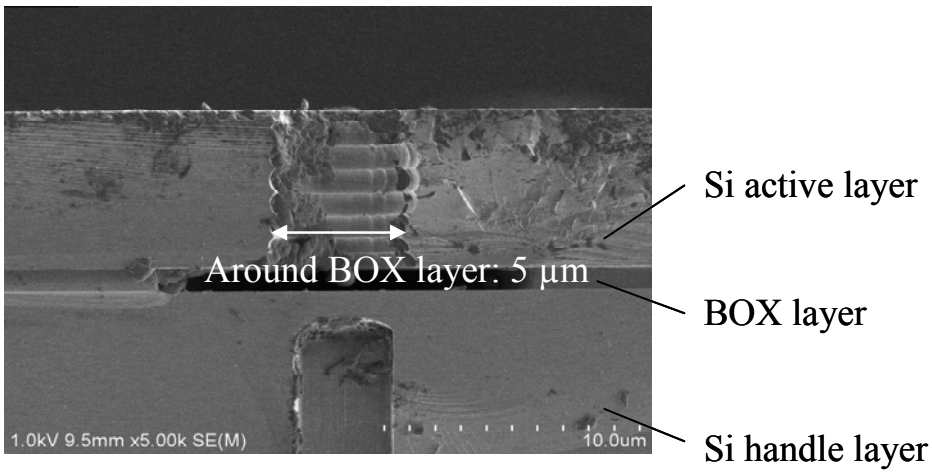
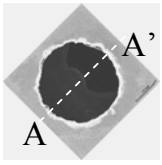
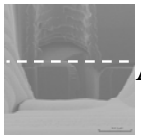
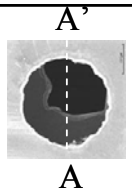
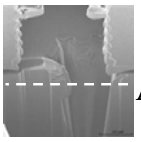
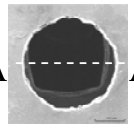
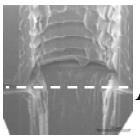


Fig.2.16 Extended cross-sectional view of the wafer, observed near the BOX layer of an SOI wafer. (the central part of the wafer)

Table 2.7 Diameters and positioning accuracies of three holes in an SOI wafer.

	Top view	Cross-sectional view	Hole diameter at active layer [μm]	Hole diameter at support layer [μm]	X-way tilting [μm]	Y-way tilting [μm]
U			6.83	3.86	1.79	1.79
C			6.08	4.55	1.05	1.35
L			6.40	5.66	0.10	0.99

When noting X and Y deviations in a wafer-planar direction, it was found that the hole position deviations at the Upper, Center, and Lower (represented respectively by U, C, and L in the figure) parts on the active and handle layers were not uniform. The cause of the uneven deviations seems to be a tilted etching shape owing to dry etching.

Dry etching is a method for applying power to an etching gas species to make it plasma, which then etches the wafer. When a bias power is applied to the bottom of the wafer during this process, an electric field is generated and positive ions in the plasma go straight to the wafer. Positive ion components that enter the wafer periphery are somewhat angled due to the difference in hole diameter between the plasma generation location and the wafer periphery.

By referring to the data available from the equipment manufacturer, the angles of etching shapes when observed in the radial direction of the wafer can be estimated. The result demonstrated that the maximum tilting angle was 0.2° when dry etching was applied to a 4-inch wafer.

As shown in Figure 2.17, when though-holes with a 250-μm diameter is proccessed in the Z direction, the maximum tilting may be X = 250 μm x tan(0.2°) = 0.87 μm in the direction of positional deviation.

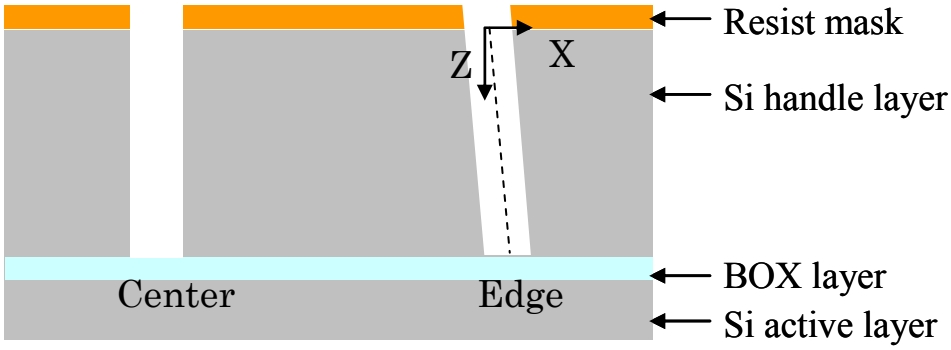


Fig.2.17 Schematic illasuration of substrate tilted by dry etching.

If the deviation at Center is assumed to be 0 considering that it is caused by factors relating to the exposure apparatus, the deviations at Upper and Lower due to tilting can be obtained. The results of the tilting angles calculated from deviations are shown in Table 2.8.

From the table, dry etching onto the handle layer causes a tilt of 0.2 ± 0.03°. Before hole-to-hole positional deviations within the wafer plane can be unified, it is necessary to improve the processing equipment so that tilting involved in dry etching will be eliminated or to compensate for positional deviations when designing the mask.

Table 2.8 Tilting angles calculated from deviations at measurement points (Upper and Lower).

	X-way tilting (μm)	Y-way tilting (μm)	$\sqrt{(X^2+Y^2)}$ (μm)	Tilting angle (°)
U	0.74	0.44	0.86	0.197
L	-0.95	-0.36	1.02	0.233

2.4 Low temperature insulator deposition

In order to form signal interconnections, an insulation film is required between the metal used for the signal interconnection in the high-aspect-ratio hole and the Si section of the substrate. Thermal oxidation is known as a method that can be used to form an insulation film on the side walls of high-aspect-ratio through-holes. However, assuming thermal oxidization heats up to 1000°C, this method is difficult to apply to form an insulation film after piezoresistors and aluminum interconnections are formed.

Therefore, a tetraethoxysilane (TEOS) dioxide film formation technology was developed by using O_3-TEOS, PECVD equipment and Precision 5000 Mark-II manufactured by Applied Materials, Inc. (Figure 2.18), as a technology that forms an insulation film at low temperature [6-7]. Researches on silicon dioxide film formation using TEOS have been made as a method to create an even film at low temperature [8-10]. By designing the conditions from the parameters for representing equipment temperature, gas pressure, and elaborating the wafer holder shape in order to optimize the TEOS gas flow and reaction, the conditions was obtained for enabling even application over the range from top to bottom of through-holes at low gas pressure. Table 2.9 shows the film formation conditions used to form films using the TEOS method.

Fig.2.18　Photograph of Plasma-enhanced CVD equipment for TEOS silicon dioxide film formation.

Table 2.9　Conditions for TEOS silicon dioxide film formation.

TEOS flow rate	3000 sccm (He)
O_3 flow rate	5000 sccm (12%w)
Susceptor head distance	6.3 mm
Film formation pressure	5 ～ 450 Torr
Film formation temperature	360 ～ 400 °C

Figure 2.19 shows the distribution of through-hole thicknesses measured in the direction of through-hole depth.

The Y-axis represents the depth of the through-hole and X-axis represents the film thickness. The graph shows that the TEOS silicon dioxide film is formed to a depth of 100 μm when the film formation temperature is lower.

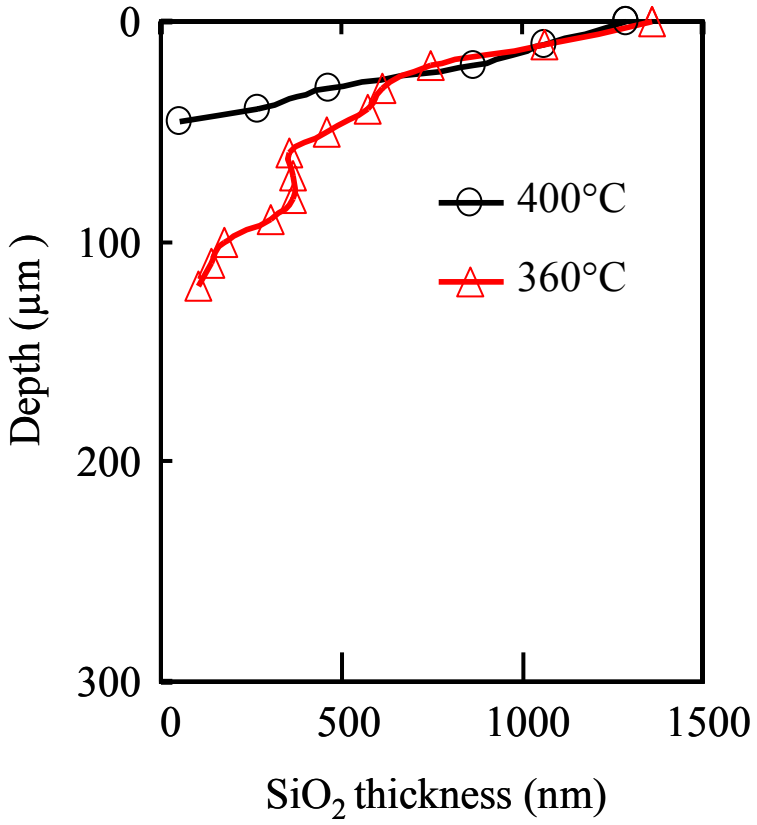


Fig.2.19 Distribution of TEOS silicon dioxide film thickness compared against through-hole depth at two TEOS silicon dioxide film formation temperatures.

The film formation pressure was also studied as an essential factor. Figure 2.20 shows the through-hole film thickness distribution measured in the direction of through-hole depth vs. the film formation pressure. The graph

shows that the TEOS silicon dioxide film is formed to a depth of 300 µm when the film formation pressure is less than 100 Torr (13.3 kPa).

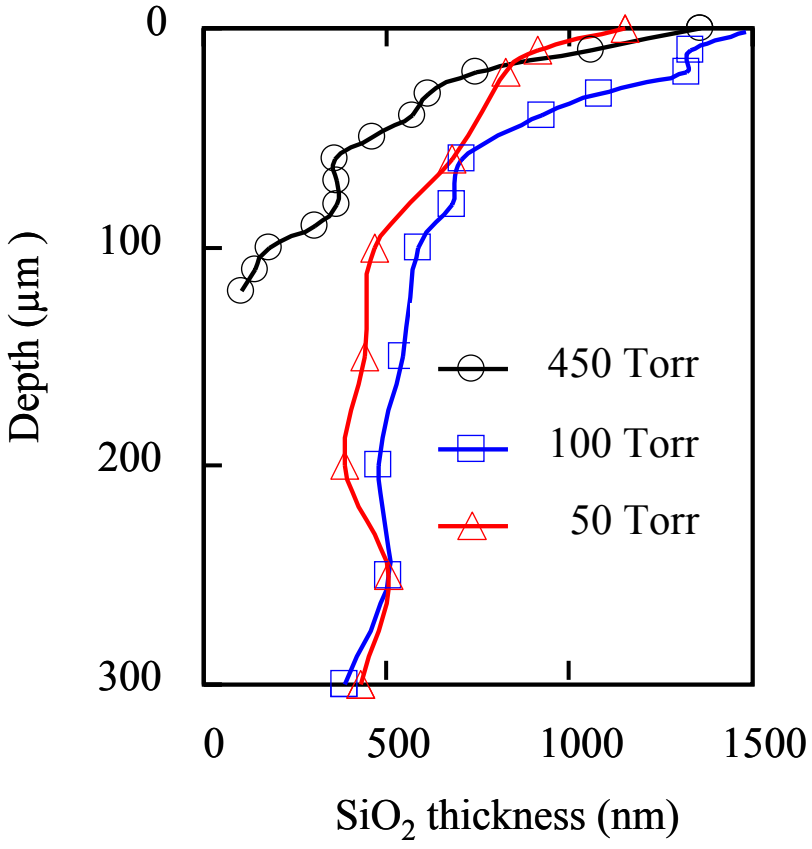


Fig.2.20 Distribution of TEOS silicon dioxide film thickness compared against through-hole depth at three TEOS silicon dioxide film formation pressures.

Figure 2.21 shows a cross-sectional view of through-holes after the formation of the TEOS silicon dioxide film of a 10-µm diameter through-hole in a 400-µm-thick wafer. The TEOS silicon dioxide film was obtained almost even thicknesses of 800, 600 and 750nm as observed in the direction of gas injection.

It seems that under these conditions, due to the low quantity of materials for TEOS silicon dioxide film, collision of material gases and intermediates does not occur and the mean free path is extended so that film forms into deep side-wall areas.

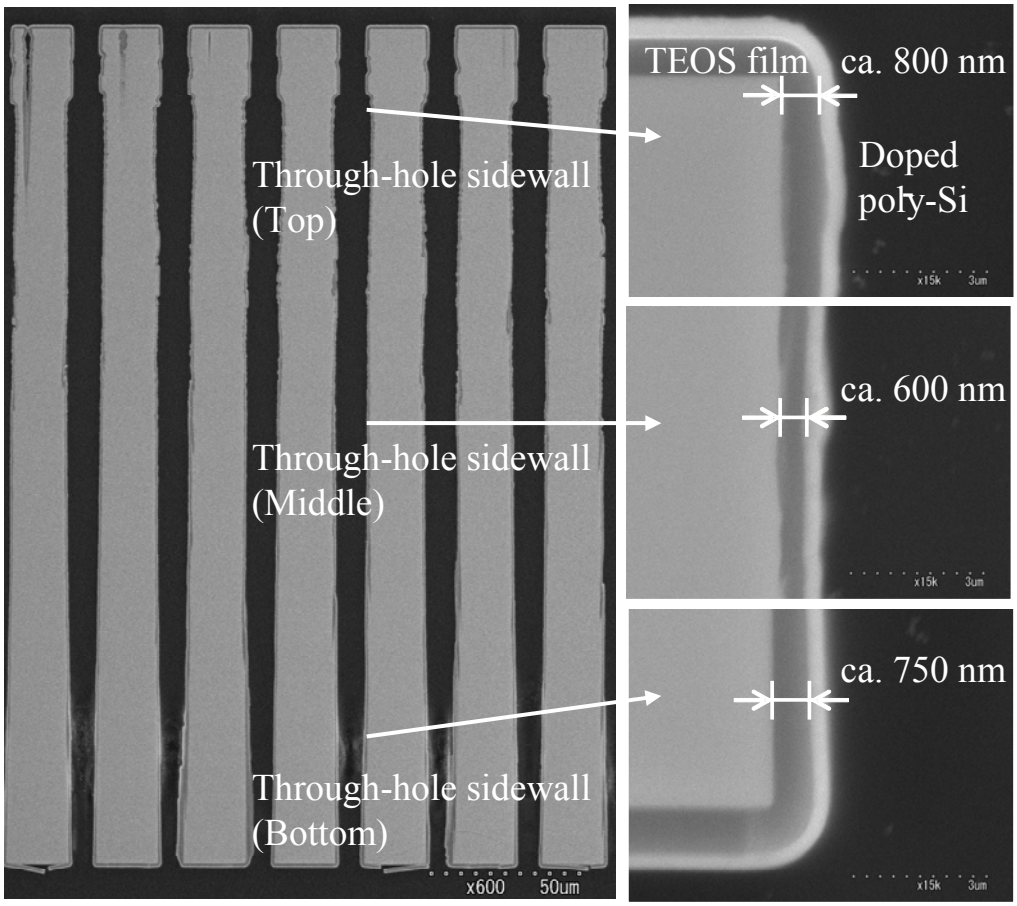


Fig.2.21 Cross-sectional views of through-holes (with a 10-μm diameter) with silicon dioxide film formed.
(wafer thickness: 400 μm)

In addition, Figure 2.22 shows the result of forming a TEOS silicon dioxide film on an SOI wafer that includes the formation of 5-μm diameter

through-holes.

It was confirmed that the silicon dioxide film was formed enough though the thickness of the TEOS silicon dioxide film tends to thin in the middle part compared with the through-hole of 10-μm diameter. Moreover, the formation of the TEOS silicon dioxide film of the BOX layer neighborhood is shown in Figure 2.23.

The TEOS silicon dioxide film of 500 nm was formed with shape with which it covered enough almost uniformly though the BOX layer was shape that the etching was growing compared with the active layer and handle layer.

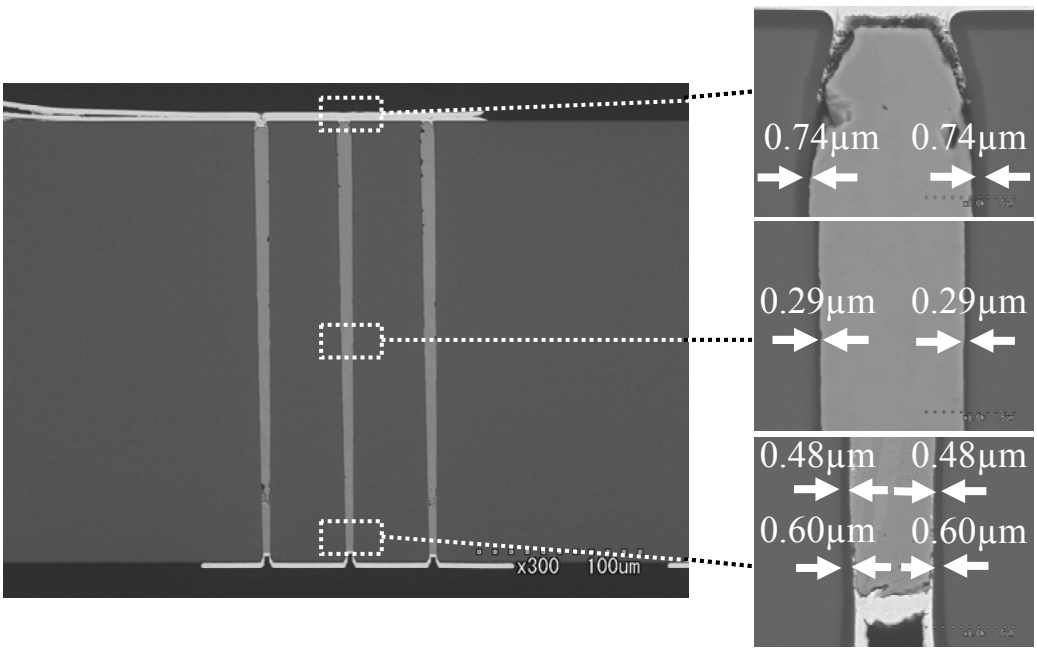


Fig.2.22 Cross-sectional views of an SOI wafer through-hole (with a 5-μm diameter) with TEOS silicon dioxide film formed.

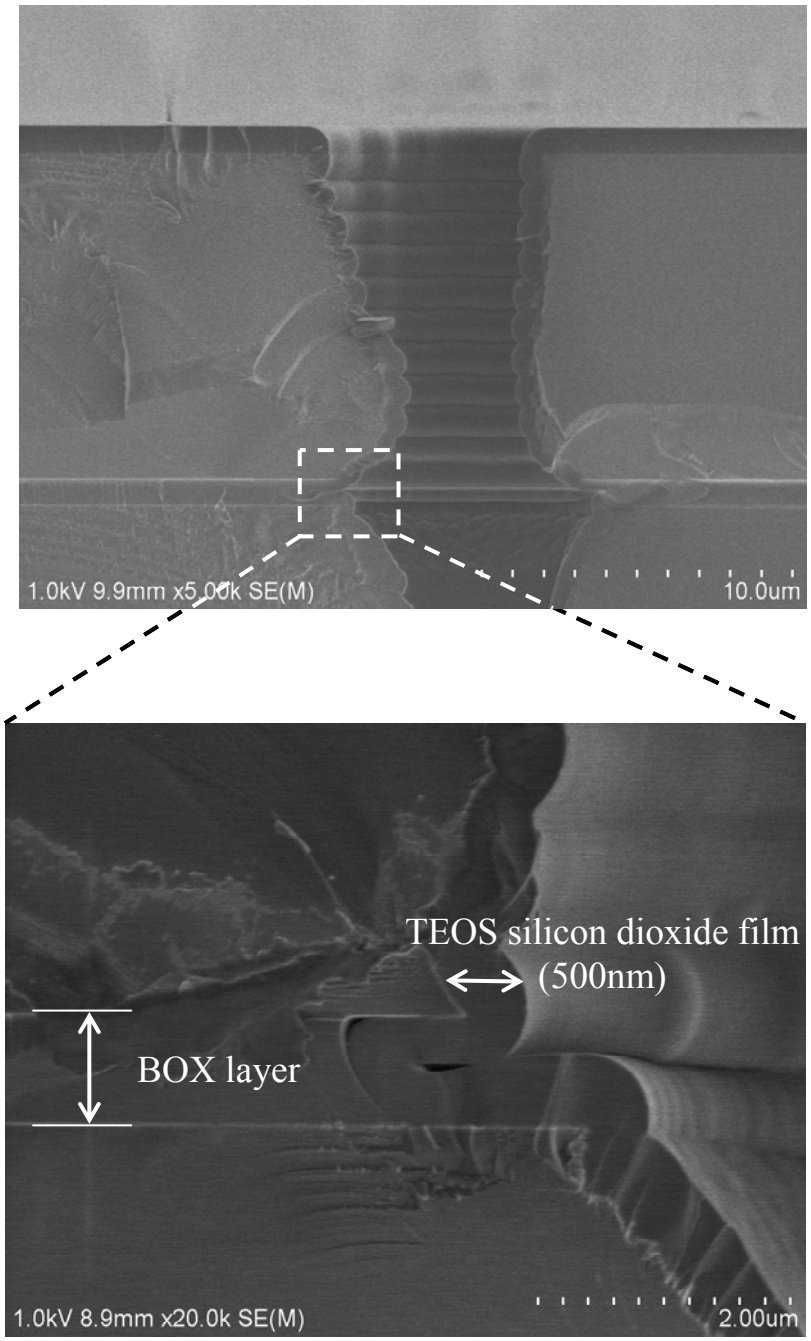


Fig.2.23 Cross-sectional views of a 5-μm diameter SOI wafer through-hole with TEOS silicon dioxide film formed, observed near the BOX layer.

2.5 Conclusion

This chapter has described that for the assumed practical level of through-holes MEMS device wafers in infrared sensor arrays, through-holes with diameters of 5 μm and aspect ratios of at least 50 are to be achieved, and that the individual processes obtained through development efforts for the formation of through-holes were proven at a practical level. Further details are as follows:

(a) First, thick-film resist formation technology and dry etching technology based thereon were studied as candidate technology for high-aspect-ratio dry etching. The resulting technology proved to be successful in forming vertical holes with a diameter of 5 μm and an aspect ratio of 50 in a 250-μm-thick silicon wafer.

(b) Second, the result of a double-side etching method to form through-holes with a 5-μm diameter and 52:1 aspect ratio in SOI wafers, the use of which is extending to MEMS devices has been presented, along with technical view concerning positioning accuracy as the problem to be solved for better through-hole formation by double-side etching on SOI wafers.

(c) Finally, TEOS silicon dioxide film formation technology based on PECVD using an O_3-TEOS gas has been proposed as a method that can be used to form an insulation film for created through-holes. By designing the conditions from the parameters for representing equipment temperature, gas pressure, and elaborating the wafer holder shape in order to optimize the TEOS gas flow and reaction, it has been demonstrated that a uniform 500-nm TEOS silicon dioxide film can be formed all over the through-hole side wall.

References

[1] S.Sasaki, T.Seki, M.Oba, K.Imanaka, T.Toriyama, T.Miyano, M.Kimata, and S.Sugiyama, Proc. the 24th Symposium on Sensors, Micromachines & Applied Systems, **433**, 2007

[2] K.Hosoya and M.Oba, Omron Technics, Vol.36, No.2, **130**, 1996

[3] T.Suemasu, K.Itoi, S.Yamamoto, and T.Takizawa, Fujikura Technical Review, No.102, **53**, 2002

[4] H.Ikeda, M.Kawano, and T.Mitsuhashi, SEMI STS symposium 2005, **9**, 2005

[5] I.Miyazawa, K.Matsui, K.Hara, Y.Matsuo, M.Ishii, and Y.Yokoyama, Proc. Int. Conf. on Electronic Packaging (ICEP), **320**, 2003

[6] A.Kanai, M.Moriguchi, S.Sasaki, and M.Oba,The Institute of Electronics, Information and Communication Engineers (IEICE), Vol.J92-C, No.11, **640**, 2009

[7] A.Kanai, S.Sasaki, and M.Oba, Proc. The 25th Sensor Symposium on Sensors, Micromachines & Applied Systems, **117**, 2008

[8] J.Huang, K.Kwok, D.Witty, and K.Donohoe, J.Electrochem, Vol.140, Issue 6, **1682**, 1993

[9] E.Sleeckx. M.Schaekers, and E.Durr, ECS Trans. Vol.25, Issue 8, **659**, 2009

[10] H.Kotani, NEW GLASS 35, Vol.9, No.4, **14**, 1994

Chapter 3

Design and fabrication of through-hole interconnection

3.1 Introduction

This chapter describes the technology used to form interconnections through the filling of the through-holes studied in Chapter 2 with conductive material.

After studying various interconnection formation methods, it was judged that the development of the following two approaches would be reasonable. This was because, for the wafer-through interconnection to be performed, the specifications to be fulfilled differed in interconnection formation process between the two approaches: the Via-First approach [1] applied at the early stage of the process, or the Via-Last approach [2] applied at the later stages of the process. Table 3.1 lists through-hole interconnection formation methods. The evaluation criteria for selecting a high-speed, high-stability, and low-cost interconnection formation is as follows:

a) Track record of high-aspect-ratio formation.
b) Process temperature.
c) Throughput (speed).
d) Signal interconnection quality (resistance).
e) Past record (reliability).
f) Affinity with MEMS process.
g) Equipment cost.

When the contamination inside equipment becomes several problems in addition to above evaluations, it is necessary to take into consideration that the metal through-hole interconnection cannot be formed before such as CMOS process and other semiconductor processes.

Table 3.1 Comparison of various through-hole interconnection formation methods.

	Bottom-up plating	Damascene	Doped poly-Si	Electroless plating	MO-CVD +Damascene	PECVD	Cat-CVD
Aspect ratio (AR)	◎ ～AR50	× ～AR10 (＊1)	△ ～AR25	△	△	△	△
Temperature	○ ～50°C	○ ～50°C	× 600°C	○ ～50°C	○ ～50°C	△ 300°C	△ 250°C
Rate	△ 10μm/h	○ 30μm/h	△ <1μm/h	× <0.1μm/h	○ 30μm/h	△ <1μm/h	△ <1μm/h
Interconnection resistance	○ <1Ω	○ <1Ω	○ <150Ω	○ <1Ω	○ <1Ω	○ <10Ω	○ <10Ω
Reliability	△	◎ (＊2)	◎ (＊2)	△	△	△	Unknown
Process affinity	△	◎ (＊2)	◎ (＊2)	△	△	△	△
Equipment cost	○ (＊3)	○ (＊3)	○ (＊3)	○ (＊3)	× (＊4)	× (＊4)	× (＊4)

(*1): Limited by plating solution

(*2): Use for DRAM etc.

(*3): Less than some ten million yen

(*4): Over 100 million yen

These interconnection formation methods were assessed by the light of the above seven criteria. Based on the results of this assessment, it was decided to implement development of the bottom-up plating method and doped poly-Si method for adoption to high aspect ratios. The reason why two types of

process were selected was that the interconnection specification depended on the device type.

In the case of through-hole interconnections for the output from infrared MEMS array sensors, for example, the doped poly-Si method will cause no problem because, considering that the resistance of one thermocouple is about tens of kilo-ohms, the voltage drop across a through-hole interconnection with a resistance of several kilo-ohms resistance is low. The power consumption does not increase either because the current of a latter-stage amplifier circuit, such as an operational amplifier, is several tens of nano-amps. However, power line and grounding interconnections for IC need a larger current. Therefore, the bottom-up plating method, which produces low-resistance metal interconnections, is more suitable.

3.2 Interconnection formation by bottom-up plating method

The major challenge for bottom-up plating technology development is to establish a method of forming a seed layer to enable plating growth. Since the Cu plating process occurs as a reaction between the plating solution and the interface where charges are supplied, it is necessary that the seed layer should only be formed on areas where Cu growth is desired. Figure 3.1 shows a basic process of bottom-up plating. In this case, the Cu needs to grow inside the through-hole, starting at the bottom and proceeding upward. Therefore, contacts between the plating solution and the interconnection except at the bottom of the through-hole not only promotes Cu precipitation in such areas, but also hinder uniform Cu growth within the through-hole. Figure 3.2 shows a uneven plating caused by insufficient contact of the seed layer. The uneven Cu growth in the through-hole causes not only problem of the electrode shape but also generation of the voids, and to increase resistance.

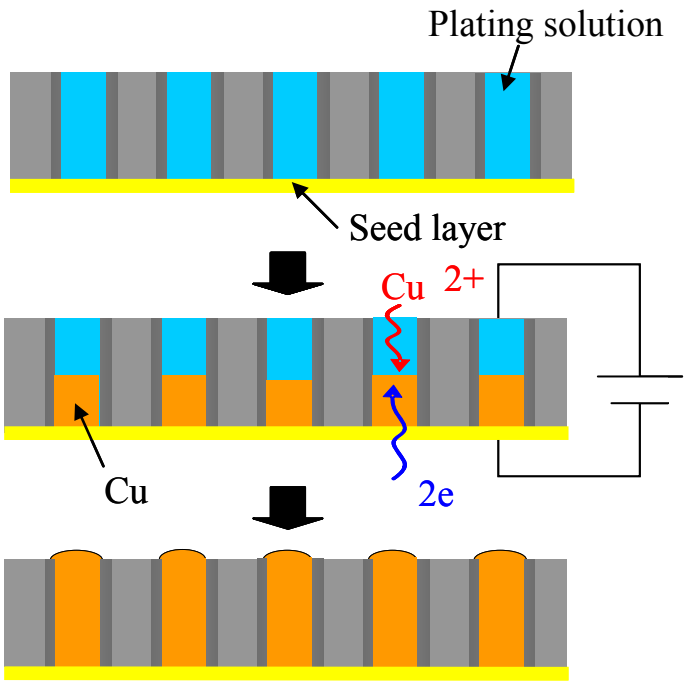


Fig.3.1 Basic process of bottom-up plating.

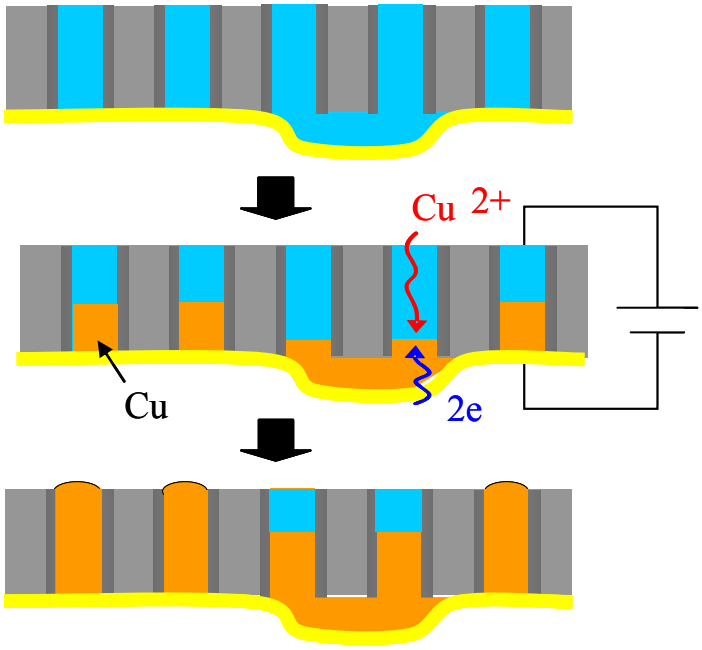


Fig.3.2 Uneven plating caused by insufficient contact of the seed layer.

There are two seed layer formation methods. The first method is to form a seed layer on the back side of the silicon wafer first and to form micro-holes by etching through the silicon substrate from the front side until the holes reach the back seed layer, and the other, is to form the micro-holes first and to form a seed layer later.

Conventional technology can be used to form a seed layer by the first method. However, this is not practical since the seed layer is damaged when the silicon substrate is etched. In addition, an insulation film must be formed on the side walls of the micro holes. If deposition is used to form the insulation film, an insulation film is also formed on the seed layer surface. This makes it difficult to apply electrolytic plating. If a thermal oxidization process is used to form an insulation film on the side walls of micro holes, the metal seed layer will be damaged. In addition, setting of any metal containing silicon substrates should be avoided as it would lead to contamination of the thermal oxidation equipment.

Therefore, through-hole interconnection formation technology was developed by first forming through-holes, and then forming the insulation and seed layers before applying bottom-up plating [3-4]. Figure 3.3 shows the through-hole interconnection formation process flow.

There is no contamination inside equipment when a deposition process and a thermal oxidation process be used, because the insulation film is formed before the seed layer formation, it becomes applicable to not only an infrared MEMS array sensor but general sensors, because the flexibility of a later process increases. Moreover, in order to plate immediately after seed layer formation, the seed layer not only does not receive the damage by etching, but the seed layer surface pollutes is lost.

On the other hand, in order to form the seed layer in the thought-hole by sputtering, the seed layer is formed only in the surface at the bottom of the silicon wafer, and the side wall near the opening of the thought-hole, and to close an opening, not formed.

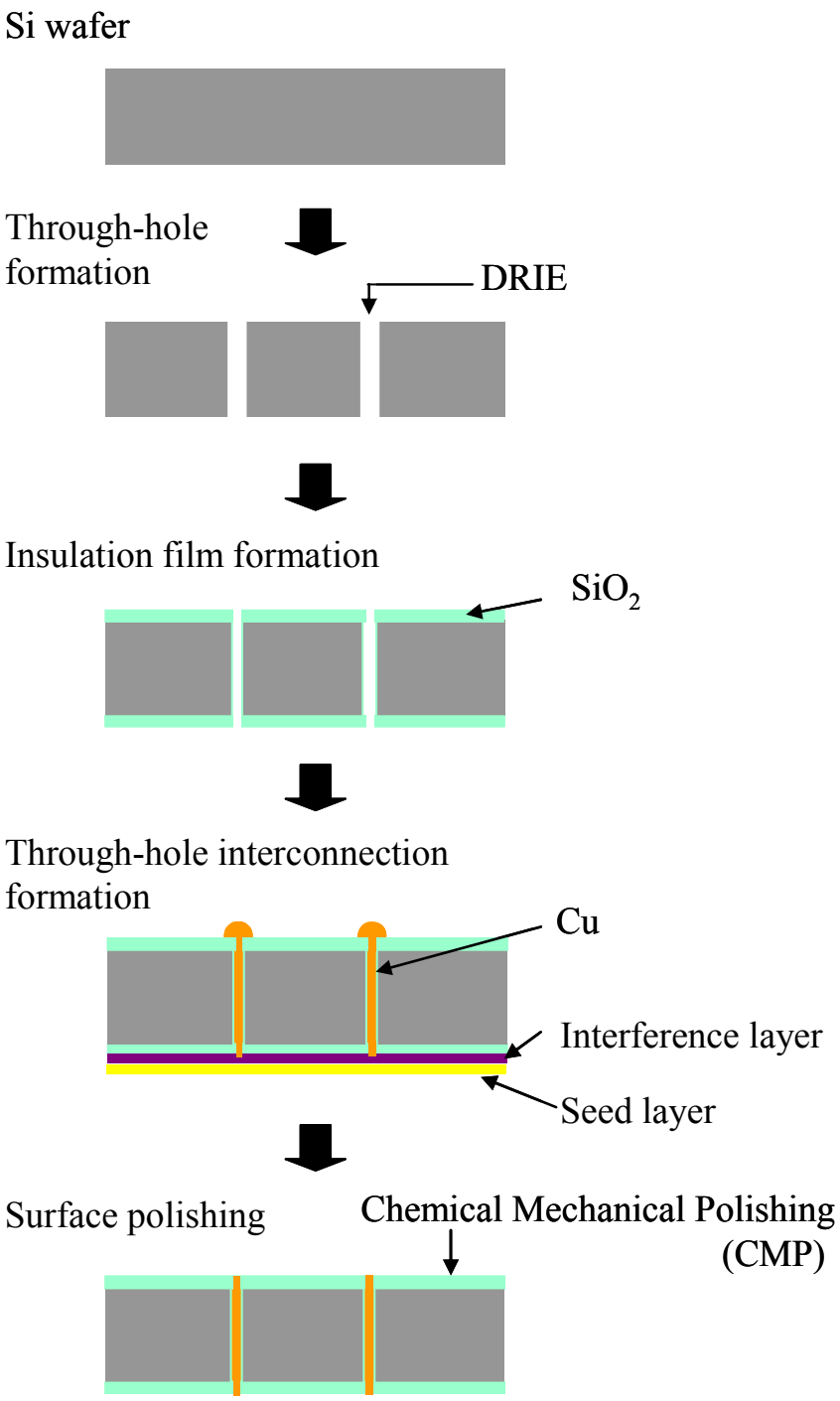


Fig.3.3 Schematic of through-hole interconnection formation process.

3.2.1 Experimental procedure

The first step is to form through-holes by dry etching and form an insulation film evenly over the side walls of the through-holes. The next step is to form a seed layer at the bottom of the through-holes and form through-hole interconnections by applying bottom-up plating. More specifically, a Cr/Au seed layer is formed by sputtering the Si substrate in which the through-holes are formed.

The conditions listed in Table 3.2 were used for bottom-up plating. The plating apparatus used was a CUP PLATTER manufactured by Electroplating Engineers of Japan Ltd. (EEJA) and the plating solution used was MICROFAB Cu300 of EEJA.

Table 3.2 Bottom-up plating conditions.
(Cu Plating Solution: MICROFAB Cu300)

Solution temp [deg]	Target thuckness [μm]	Current [mA]		Volt [V]	Flow rate [L/min]
25	525	1st.	0.5	0.1	25
		2nd.	1.3	0.4	25

Control of any excess Cu extruding from the through-holes following the bottom-up plating process would be difficult by only the plating conditions, so any excess was flattened by chemical mechanical polishing (CMP).

Figure 3.4 is a photograph of the bottom-up plating apparatus and Figure 3.5 is a photograph of the wafer loading unit in the bottom-up plating apparatus.

Fig.3.4 Photograph of the bottom-up plating apparatus.

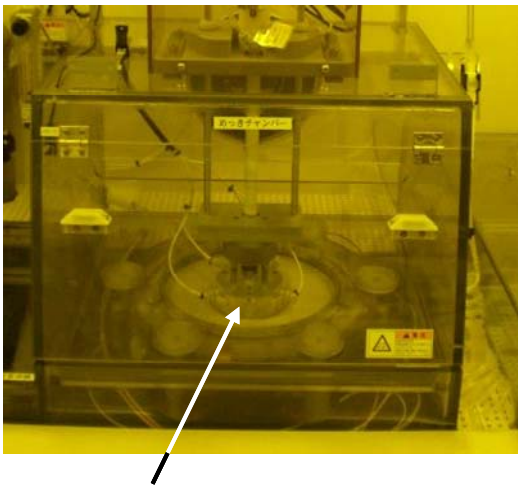


Fig.3.5 Photograph of wafer loading unit of the bottom-up plating apparatus.

Since the aspect ratio achieved by this method is considerably higher than 50, which is the aspect ratio of damascene and other interconnections formed by conventional plating methods, slight differences in current density distribution, plating solution concentration, and/or other quantity might influence the homogeneity of copper precipitation on the wafer. Furthermore, even if it dips the wafer with a 5-μm through-hole which formed the seed layer in plating solution, the plating solution doesn't enter the through-hole by the surface tension of solution, and it doesn't reach the seed layer of the bottom. In addition, the bottom-up plating method requires power feeding from the wafer back side as a seed layer must be formed on the wafer back.

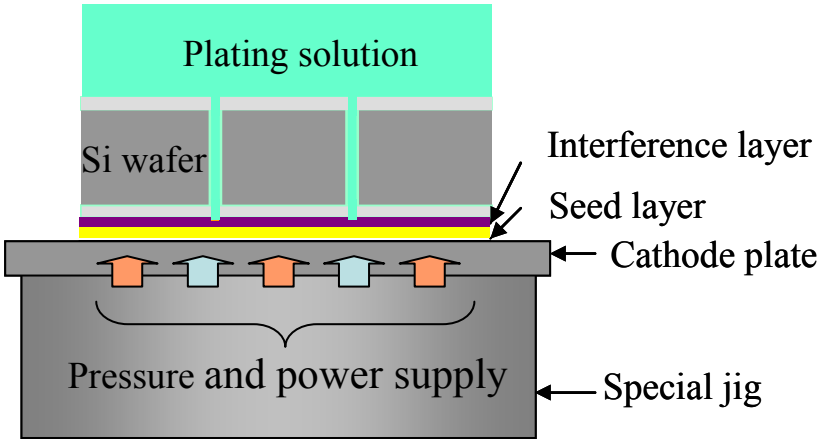
Unfortunately, since generally available plating equipment, used for the so-called damascene processes, only allows power feeding from the front side of the wafer, the development of new plating apparatus was needed to fulfill above requirements.

By thus developing new apparatus that could accomplish the following two tasks, a satisfactory bottom-up plating method that would ensure homogeneous plating was established.

1. Revise the pre-wetting process for the plating solution to assist in appropriately filling the through-holes with the plating solution for the purpose of addressing the problem of copper precipitation inhomogeneity caused by insufficient plating solution filling.

2. Develop a special jig as shown Figure 3.6 (a) that can feed power to the seed layer from the back side of the wafer and can also ensure resistance uniformity and prevent plating solution leakage, with the purpose of unifying the power feed over the entire wafer surface. Figure 3.6 (b) shows the schematic of bottom-up plating method using the developed special jig.

(a) Photograph of special jig



(b) Schematic illustration of bottom-up plating

Fig.3.6 Special jig for seed layer interconnections and bottom-up plating method using special jig.

3.2.2 Results

Figure 3.7 shows cross-sectional views of bottom-up Cu-plated 10-μm diameter through-hole interconnections that are formed at a minimum pitch of 30 μm in a 525-μm-thick wafer that is sputtered with Cr and Au to form a seed layer whose Cr thickness is 0.05 μm and Au thickness is 0.25 μm.

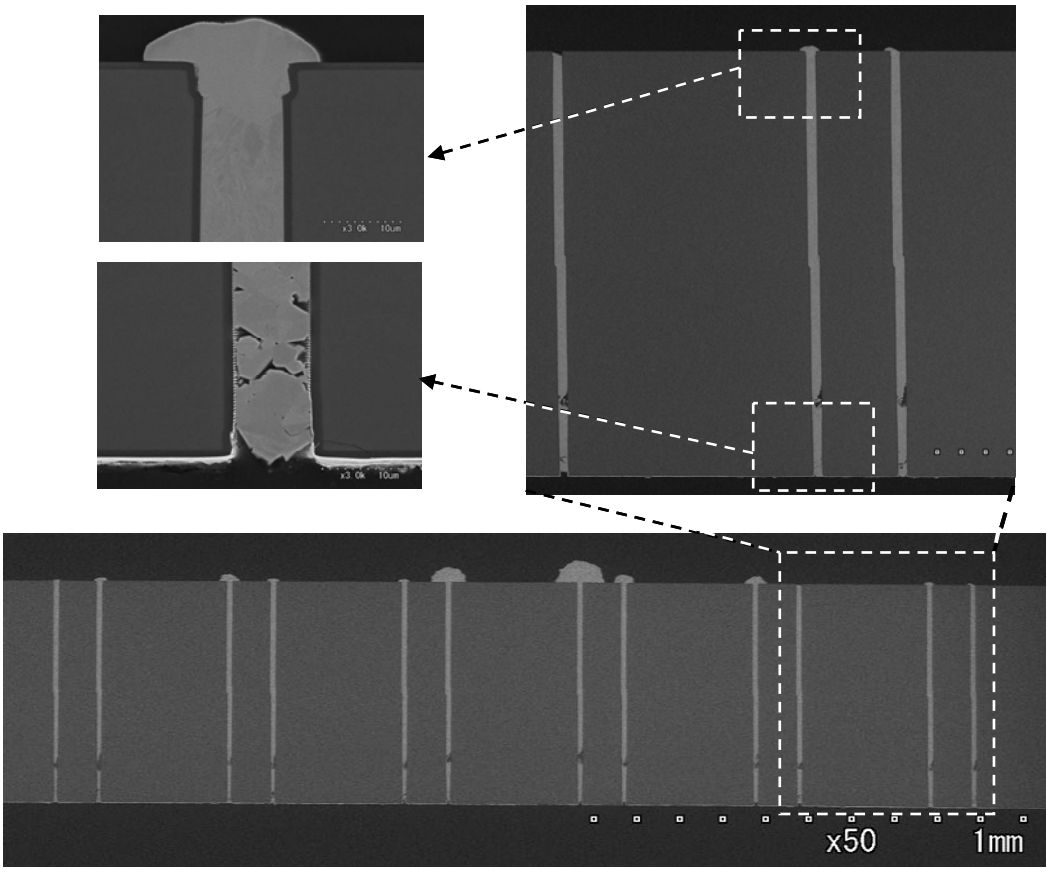


Fig.3.7 Cross-sectional views of bottom-up plated through-hole interconnections with a 0.25-μm-thick Au seed layer.
(substrate thickness: 525 μm, through-holes diameter: 10 μm)

Growth speed variations and voids in the vicinity of the seed layer are observed. It seems that as the seed layer was 0.25-μm and too thin, these observations were caused by electrolytic distribution differences due to variations in the degree of contact with the seed layer interconnection jig. It was later confirmed that this problem could be addressed by thickening the seed layer when forming 5-μm diameter through-holes.

Figures 3.8 and 3.9 show cross-sectional views of bottom-up plated through-hole interconnections formed in a wafer that is covered with a conductive-tape as a seed layer instead of Cr/Au sputtering in an effort to shorten the process. The conductive-tape was covered all over the bottom of wafer with through-holes, the conductive-tape was stuck to the jig for bottom-up plating, it put into plating solution, and bottom-up plating was performed. These photographs show that the plating is free of voids. Moreover, when the wafer bottom is observed, it turned out that Cu was plated so that all at the bottom of wafer might be covered. It was considered that plating solution entered and was plated Cu between the conductive-tape and wafer during plating.

However, it was found that this method requires further improvement for practical application because the tape will leave its residues upon removal after the plating process.

Metal interconnections were also formed in a 250-μm-thick Si substrate by forming 5-μm diameter micro through-holes and using the bottom-up plating method. Figure 3.10 shows cross-sectional views of these interconnections. The Au thickness of the seed layer was increased to 2 μm in order to improve the degree of contact with the seed layer interconnection jig.

As a result, metal interconnections without voids were formed in micro through-holes with a 5-μm diameter and 50:1 aspect ratio, by the bottom-up Cu plating method. Figure 3.11 shows a general view of a 4 inch wafer with through-hole interconnections.

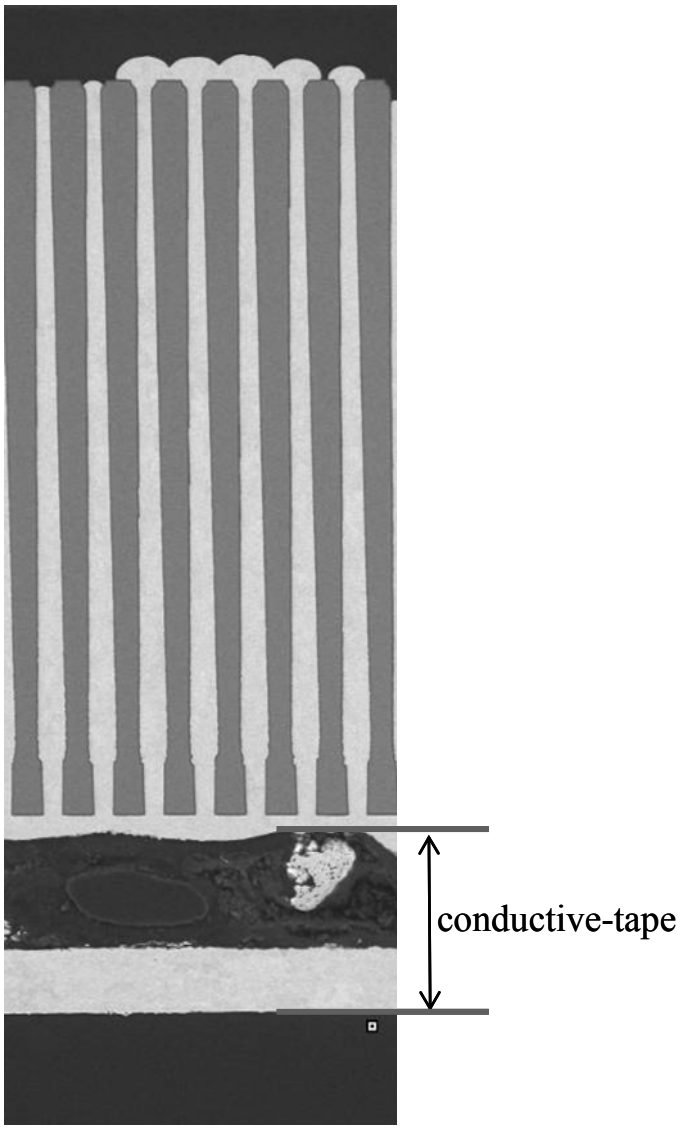


Fig.3.8 Cross-sectional view of bottom-up plating through-hole interconnections with conductive-tape seed layer.
(substrate thickness: 300 μm, though-hole diameter: 10 μm)

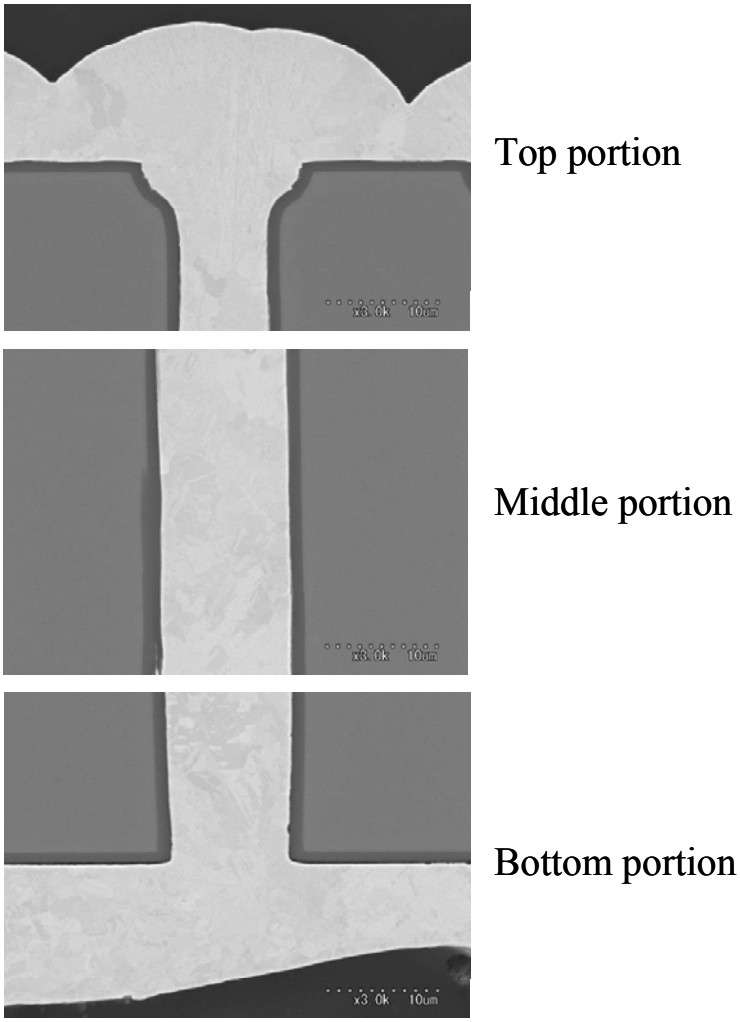
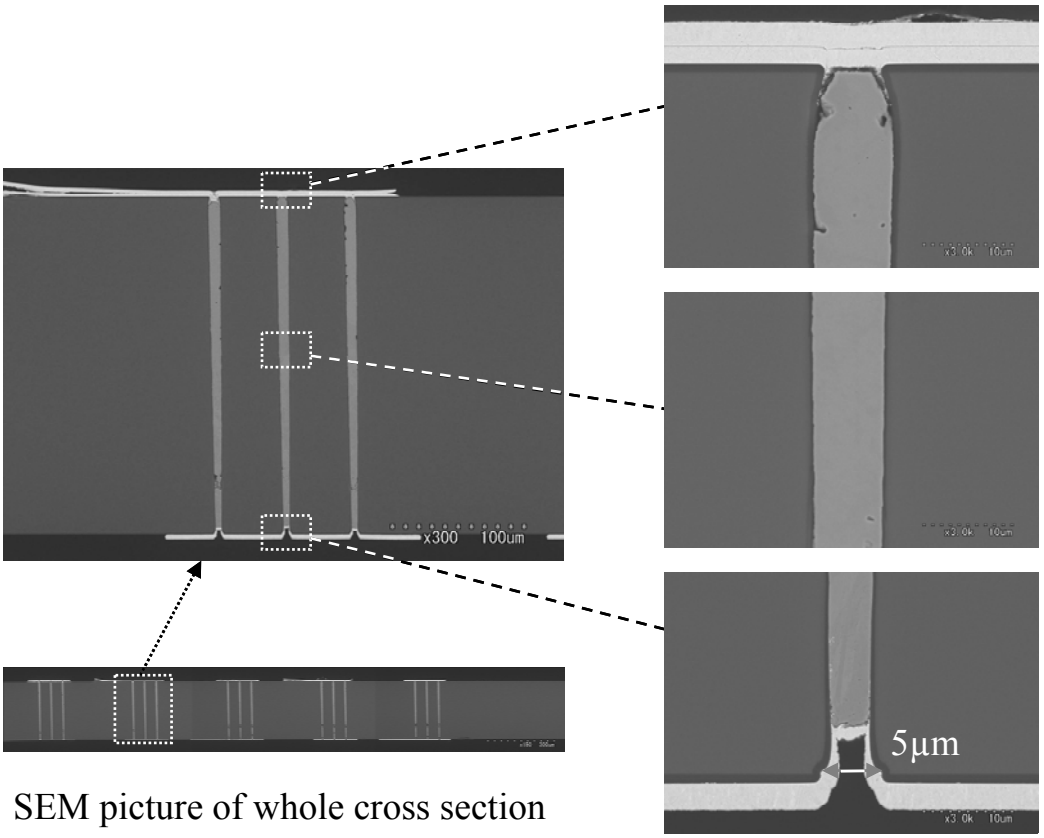


Fig.3.9 Expanded cross-sectional views of bottom-up plated through-hole interconnections with conductive-tape seed layer. (substrate thickness: 400 μm, though-hole diameter: 10 μm)



SEM picture of whole cross section

Fig.3.10 Cross-sectional views of bottom-up plated through-hole interconnections with 2-μm-thick seed layer.
(substrate thickness: 250 μm, through-hole diameter: 5 μm)

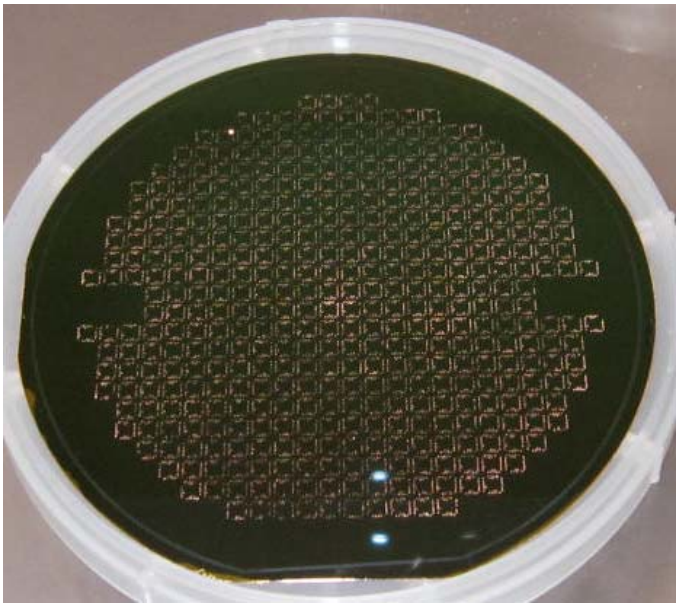


Fig.3.11 General view of 4 inches wafer with through-hole interconnections.

The resistances of the though-hole interconnections were measured to assess the electric continuity of these interconnections. As shown in Figure 3.12, through-hole and planar interconnections were daisy-chained so that they were connected in series and measured the resistance of eight interconnections connected in series and the resistance of two sets connected in series, each containing eight interconnections connected in parallel using a four probe terminal resistance measurement method. By subtracting the resistance of the planar connections that lie on the substrate from the measured resistance of the test element group (TEG) interconnection mounted on the substrate, the through-hole interconnection resistance was calculated.

From the results of measuring the through-hole interconnections shown in Figure 3.7, the resistance of each interconnection was found to be 3.36 to 141 ohms as indicated in Table 3.3. This range of resistance is between 18 to 77 times rather than the calculated theoretical value of the resistance, 0.18 ohm, of each interconnection, taking into account the values of the length and diameter of each through-hole and the resistivity of Cu. It is suggested that

these high resistance values be caused by narrower effective interconnection diameters due to the existence of voids.

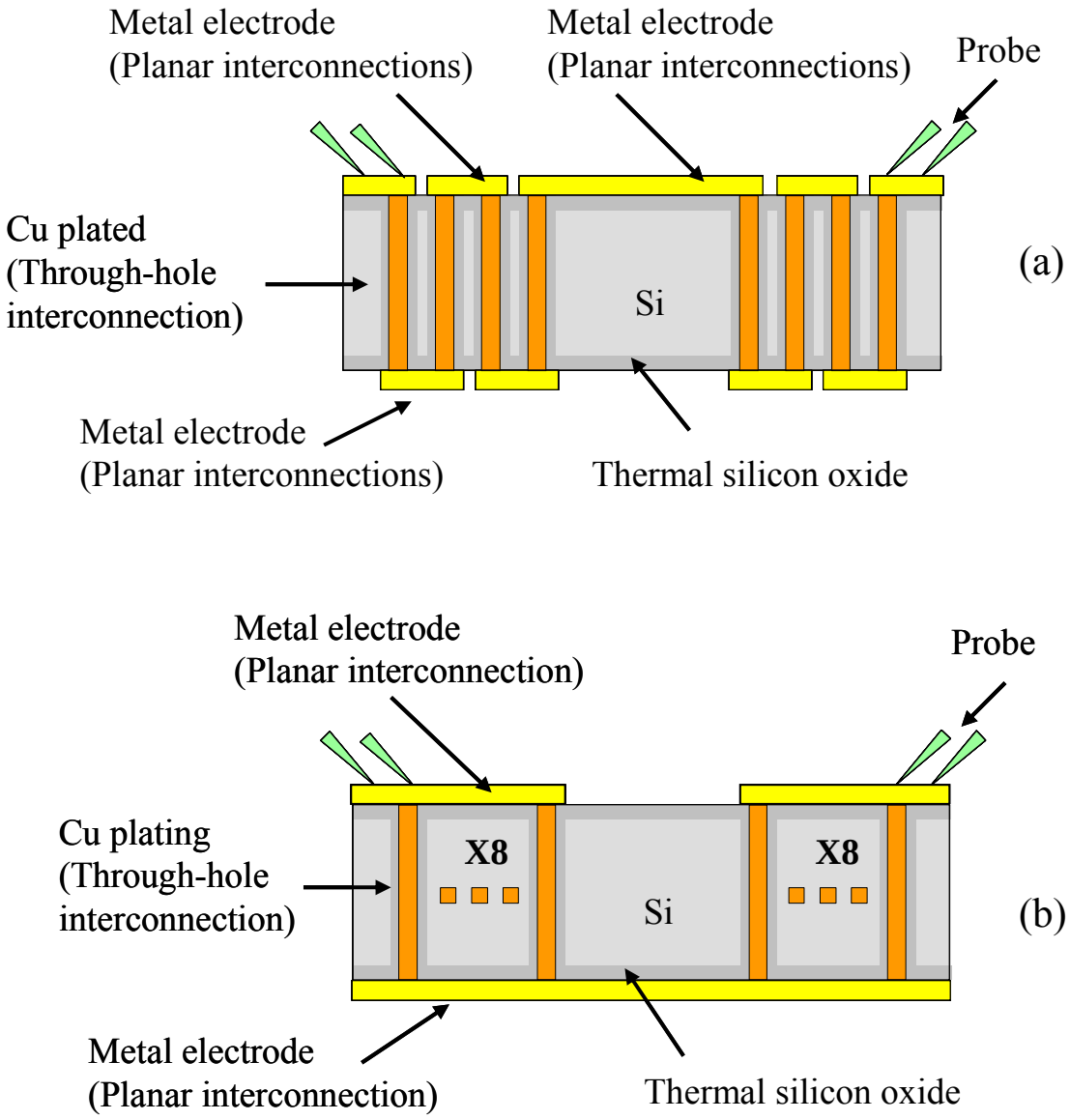


Fig.3.12 Schematic of through-hole interconnection resistance measurement method; (a) Eight through-hole interconnections are connected in series, as for this, two sets to which four through-hole interconnections were connected in series are connected in series. (b) Eight through-hole interconnections are connected in parallel, and these are connected to series with two sets.

Table 3.3 Results of measuring 10-μm diameter through-hole interconnections with voids as shown in Figure 3.7. (Thickness: 525 μm)

	Total resistance [Ω]	Planar interconnection resistance [Ω]	Measured resistance of one interconnection [Ω]	Theoretical resistance of one interconnection [Ω]
8 in series	115	188	141	0.184
8 in parallel 2 in series	0.64	0.22	3.36	

Table 3.4 shows the results of measuring 5-μm diameter, 250-μm-thick void-less through-hole interconnections with a seed layer whose Au thickness was increased to 2.0 μm (shown in Figure 3.10). The resistance of eight interconnections connected in parallel was found to be 0.21 ohm, which is close to the theoretical bulk interconnection resistance of 0.18 ohm.

Table 3.4 Results of measuring 5-μm diameter void-free through-hole interconnections (shown in Figure 3.10). (Thickness: 250 μm)

No.	Resistance of 8 in parallel 2 in series interconnection [Ω]	Resistance of one interconnection [Ω]
1	0.25	2.0
2	0.20	1.6
3	0.19	1.5
4	0.22	1.8
5	0.21	1.7
Average	0.21	1.7

3.3 Interconnection formation by doped poly-Si method

This section describes the through-hole interconnection formation technique based on the doped poly-Si method that allows signal interconnections to be formed using the Via-First approach.

Doped poly-Si is used as a material of the thermopile using the Seebeck effect in the MEMS device besides being used as a lot of element materials in the MOS process, and applied to the infrared sensors and the flow sensors. Although through-hole interconnections which applied doped poly-Si were reported, hole diameter was 20 μm and aspect ratios also 10 to about 20 [5-6].

The doped poly-Si process is used to form a poly-Si film while adding high-concentration p-type impurities and thermally diffusing the impurities to form a low-resistance film as shown Figure 3.13.

The basic process of doped poly-Si is formed of thermal decomposition of SiH_4 by LPCVD and, for the process conditions, heats a wafer in 570°C and deposits poly-Si, doping phosphorus for the pressure in furnace to SiH_4 at 80 Pa. If pressure is lowered, deposition speed will become fast, but resistivity becomes the tendency to lower. This is because doped poly-Si is in a high density under low pressure condition. The poly-Si which deposited is to make annealing in a high temperature state at 1050°C in nitrogen gas, when was crystallized, carrier mobility will becomes fast and resistivity will decrease.

Since there is a limitation to resistance reduction with materials produced by this method, and it is difficult to use these materials for power interconnections, however the materials can be extensively used for signal interconnections.

This application is promising because if through-hole interconnections are buried in a silicon substrate before a MEMS structure is formed, the device can be produced with almost no need for later MEMS process changes.

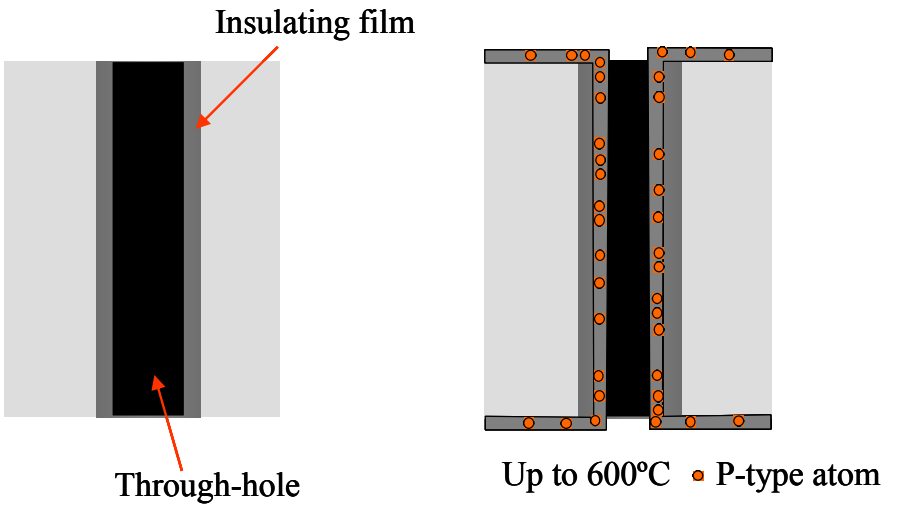


Fig.3.13 Schematic illustration of through-hole interconnection formation process using doped poly-Si method.

3.3.1 Experimental procedure

To deposit doped poly-Si, low pressure CVD (LPCVD) equipment (VERTEX DJ-802V by Hitachi Kokusai Electric Inc.), was used. Figure 3.14 shows the exterior of this equipment.

Fig.3.14 Exterior of doped poly-Si equipment.

The main process conditions were as follows: Furnace temperature of 570°C, pressure of 80 Pa, SiH_4 flow rate of 600 sccm, PH_3 flow rate of 8 sccm, and deposition time of 1 hour, then a 100-min anneal at 1050°C to fully drive dopants throughout the poly-Si. This high temperature step, like the others, also serves to relieve stress in the thick doped poly-Si film.

3.3.2 Results

Figure 3.15 shows cross-sectional view of interconnections formed in 10-µm diameter, 400-µm deep through-holes. The figure demonstrates that the doped poly-Si film thicknesses vary little, between 350 nm to 400 nm at the top, middle, and bottom levels of the side wall. Figure 3.16 shows cross-sectional views of through-hole interconnections with a 1.5-µm-thick doped poly-Si film. As with Figure 3.15, this figure also demonstrates that an even-thickness doped poly-Si film is formed over the through-hole walls.

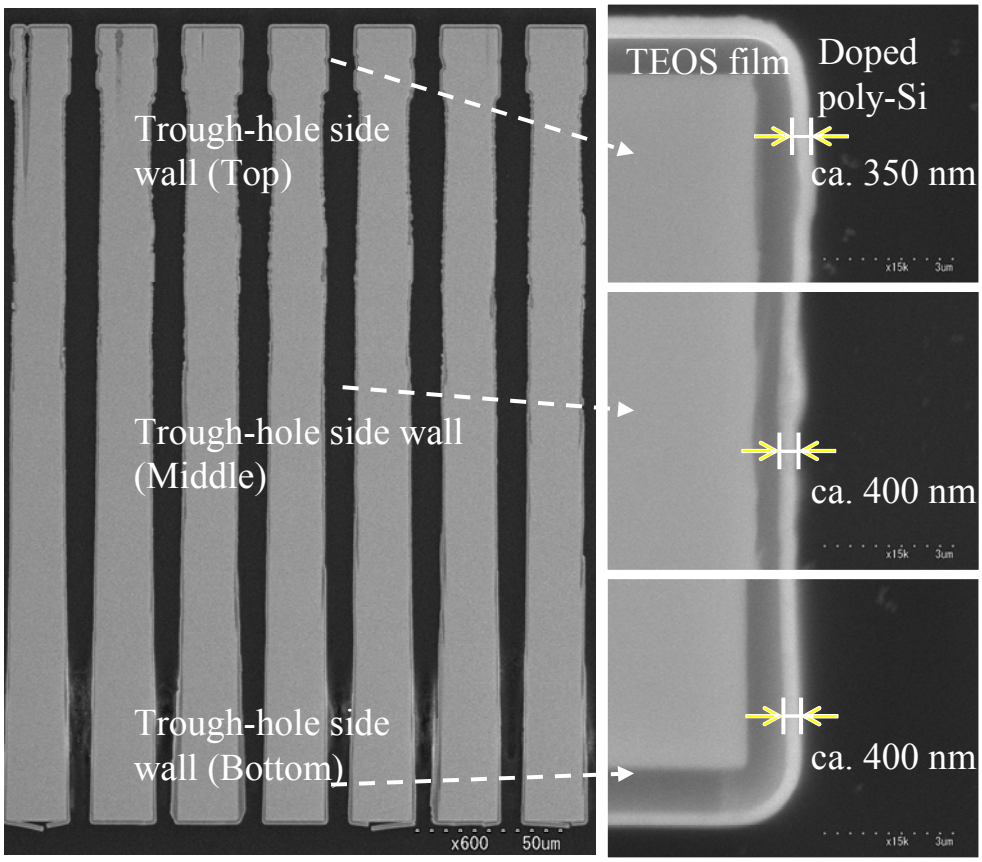
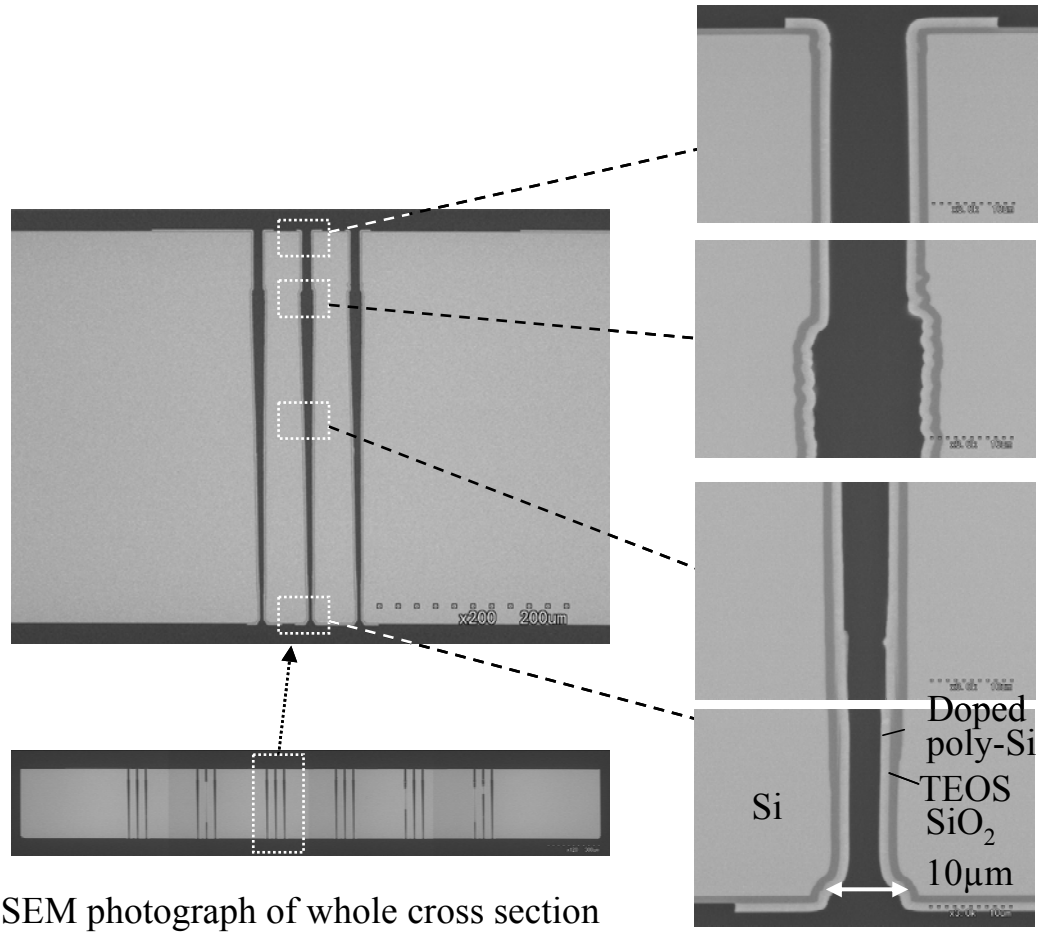


Fig.3.15 Cross-sectional views of through-hole interconnections with a deposited 400-nm-thick doped poly-Si film.



SEM photograph of whole cross section

Fig.3.16 Cross-sectional views of through-hole interconnections with 1.5-μm-thick doped poly-Si.
(substrate thickness: 400 μm, through-hole diameter: 10 μm)

The resistance of through-hole interconnections with a 1.5-μm-thick doped poly-Si film as shown in Figure 3.16, with the method shown in Figure 3.12 was measured and was obtained the following results: the resistance of eight interconnections connected in parallel was about 22 ohms, resulting in a single interconnection resistance of 177 ohms (Table 3.5).

Table 3.5 Results of measuring doped poly-Si 10-μm diameter through-hole interconnection. (thickness: 400 μm)

No.	Resistance of 8 in parallel 2 in series interconnection [Ω]	Resistance of one interconnection [Ω]
1	20.52	164.2
2	24.22	193.8
3	22.42	179.3
4	22.50	180.0
5	20.83	166.7
Average	22.10	176.8

These results match the values calculated from the measured resistivity of the doped poly-Si material, which was 1.77 x 10^5 Ωm and proved that the resistance of the through-hole interconnections is nearly equal to that of thin film interconnections, as in the case of interconnections fabricated by the bottom-up plating method.

High-sensitive infrared MEMS array sensors are characterized by a small voltage drop which is due to the fact that its resistance is sufficiently lower than several tens of kΩ, which is the resistance of one thermopile. In addition, no supply voltage is required, unlike a piezoresistive bridge. Considering these conditions, a through-hole interconnection can be judged as

sufficiently practical if its resistance is of the order of several tens of ohms. If the use of the Via-First approach for doped poly-Si is inevitable, it might be possible to increase the number of parallel interconnections to lower the resistance and/or to thin the MEMS layer to shorten the interconnection length, to ensure that the interconnections can also be used to convey power.

It should be noted, however, that interconnections, if used for infrared MEMS sensor with micromirror arrays or other similar purposes, must be hermetic. Therefore, it is necessary to ensure hermetic sealing by increasing the doped poly-Si film thickness or by forming thicker Au/Cr electrodes to close the openings. On the other hand, it was reported that micro posts of the silicon were made in the through-hole and poly-Si was buried for the aspect ratio of through-hole was about 3, the hermetic sealing was secured, and the process throughput of LPCVD was improved [7]. If the through-hole diameter is 5 μm or smaller, it can be presumed that hermetic through-hole interconnection with a doped poly-Si film can be formed more easily.

3.4 Conclusion

This chapter has reported the establishment of two technologies: the Cu interconnection formation technique based on the bottom-up plating method, which is applicable to both signal and power interconnections, and the LPCVD-based doped poly-Si method, which follows the Via-First approach with good process affinity and is particularly useful in application to signal interconnections.

As part of efforts for bottom-up plating, a seed layer interconnection jig was fabricated to apply a uniform electric field over the surface of the wafer and formed a seed layer by sputtering with Cr and Au to respective thicknesses of 0.05 and 2 μm. As a result, micro through-hole interconnections of a 5-μm diameter with aspect ratios of as high as 50:1 were obtained and it was

confirmed that these interconnections are of low resistance comparable to metal film interconnections. Conductive tape is also useful for the seed layer as a means for reducing the time required for the seed layer formation process.

The doped poly-Si was deposited onto through-holes with a 10-μm diameter with aspect ratios of as high as 40:1 by using LPCVD and was proved that the resulting interconnections were of resistances that are comparable to those of thin film interconnections.

In this study, these high-aspect-ratio through-hole interconnection formation technologies will be useful for infrared MEMS array sensor.

References

[1] E.M.Chow, A.Partridge, C.F.Quate, and T.W.Kenny, Solid-state Sensor and Actuator Workshop, **343**, 2000

[2] I.Miyazawa, K.Matsui, K.Hara, Y.Matsuo, M.Ishii, and Y.Yokoyama, Proc. Int. Conf. on Electronic Packaging (ICEP), **320**, 2003

[3] S.Lee, M.Moriguchi, S.Sasaki, and M.Oba, Electrochemical and Solid -state Science (PRiME), **2516**, 2008

[4] S.Lee, S.Sato, M.Moriguchi, S.Sasaki, and M.Oba, Proc. Int. Conf. on Electronics Packaging (ICEP), **596**, 2009

[5] E.M.Chow, V.Chandrasekaran, A.Partridge, T.Nishida, M.Sheplak, C.F. Quate, and T.W.Kenny, J. Microelectromechanical Systems, Vol.11, No.6, **231**, 2002

[6] I.Luusua, K.Henttinen, P.Pekko, T.Vehmas, and H.Luoto, Materials Research Society, Symposium. Proc. Vol.872, J5.**5**. 2005

[7] H.Ikeda, M.Kawano, and T.Mitsuhashi, SEMI STS symposium 2005, **9**, 2005

Chapter 4

Design and fabrication of wafer-level bonding

4.1 Introduction

Figure 4.1 shows a small and package-less 3D sensing module. The sensing module consists of MEMS and IC chips. In the case of MEMS part such as accelerometer, absolute pressure sensor, and infrared array sensor, vacuum hermetic sealing can be achieved by bonding IC wafer on both sides. Therefore, conventional outer vacuum package is unnecessary, and high performance in small volume can be realized. Moreover, both side ICs have common circuits for MEMS devices, and various physical quantities are able to be measured by replacing MEMS layer or stacking MEMS layers [1-2].

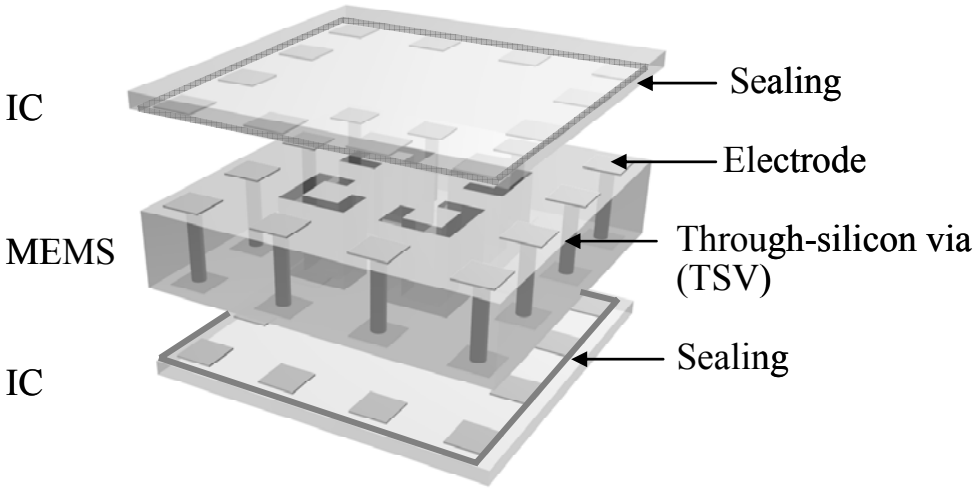


Fig.4.1 Schematic illustration of small and package-less 3D sensing module by using wafer-level bonding.

If this technology is realized, the infrared MEMS array sensor described in Chapter 1 can also make the inside of a sensor a vacuum with the structure of the sensor itself, and sensitivity not only improves, but it will be realized a vertical IC integration using through-hole interconnections is called TSV. In addition, low-temperature wafer-level bonding is required to bond sealing part for vacuum sealing and connect electrodes on both side wafers. However the wafer surface is usually covered with the hydrosphere molecules and the organic molecules after wet cleaning process, and the possibility that enough intermolecular and atom force cannot be obtained, even if wafers are bonded by the high pressure welding. In order to remove the adhesions on the wafer surface applying a high temperature for this problem, there is damage to IC when IC wafers are bonded with MEMS, and it is not possible to apply. Then, the low-temperature wafer-level bonding was required.

There are two low temperature bonding methods: low-temperature bonding using plasma surface activation and room-temperature bonding using surface activation by ion gun bombardment. The former method consists of two steps: temporary hydrogen bonding and annealing for final bonding. The latter method is direct bonding achieved by activating dangling bonds on the bonding surface. The former method might be anxious because it involves potential problems of damage to the IC layer due to annealing at 200 to 300°C and misalignment caused by the difference in thermal expansion coefficient between the materials to be bonded. Therefore, the latter method was selected. Figure 4.2 shows the exterior of the room-temperature bonding equipment (MWB-04-R manufactured by Mitsubishi Heavy Industries Ltd.), realizes room temperature wafer-level bonding. Oxidized and absorbed films are generally formed on wafer surface and stabilized. Direct bonding technology sputters the surface of wafers by ion beam and neutral atoms in vacuum atmosphere, and bonds destabilized the surfaces in room temperature by cleaning and activation, and Figure 4.3 shows the principle underlying this type of bonding.

Fig.4.2 Photograph of room-temperature bonding equipment.

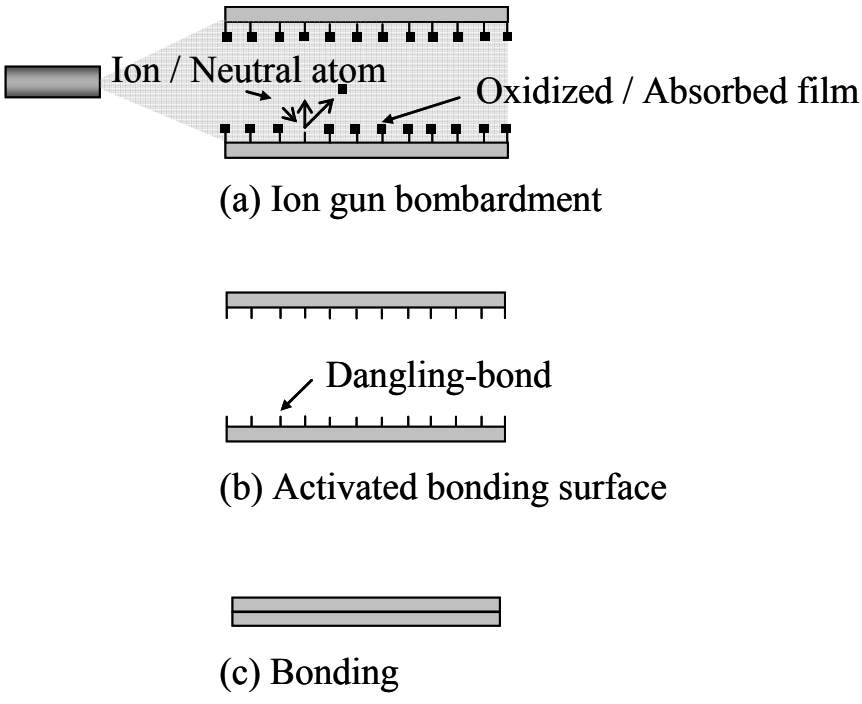


Fig.4.3 Principle of room-temperature bonding using surface activation by ion gun bombardment.

4.2 Room-temperature bonding using surface activation by ion gun bombardment

Figure 4.4 shows the test element group (TEG) to verify room -temperature bonding using ion gun bombardment for surface activation. An upper wafer was formed the alignment mark of shape to pull out in the crisscross with Al of a 100-μm length and a 100-μm width at the five places of the upper and lower sides, right and left, and the center of a wafer. A lower wafer similarly was set up the crisscross alignment mark of a 100-μm length and a 100-μm width at the position opposed to the alignment mark of an upper wafer. The Si lattice of a 50-μm width and a 3.5-μm height was located on lower wafer at intervals of 2mm. The cavity of the lattice was formed by TMAH solution in the part where the quadrangle enclosed that had been enclosed with the Si lattice corresponded to infrared MEMS array sensor.

Wafer-level bonding was tested under the room-temperature bonding conditions indicated in Table 4.1 using this TEG. The sizes of a wafer was 4 inch and 400-μm-thik double-sided mirror polished Si substrate. The TEG was assessed for bonding strength and alignment accuracy. The bonding strength of diced chips was evaluated by tensile strength test apparatus. Initial post-dicing yield was 63.5%, but it finally increased to 99.8% due to improvements, including surface roughness improvement, cleaning process changes for decontamination, and wafer warpage control.

Then, the TEG bonding status was analyzed by using infrared (IR) microscopic images and transmission electron microscope (TEM) images of wafers bonded by ion gun bombardment for surface activation. The IR image shown in Figure 4.5, when analyzed, indicates that the TEG bonding status is characterized by the fact that the bonding area increases with the bonding load.

In addition, the TEM image shown in Figure 4.6 indicates that this bonding is direct bonding without any inclusions at the wafer interface.

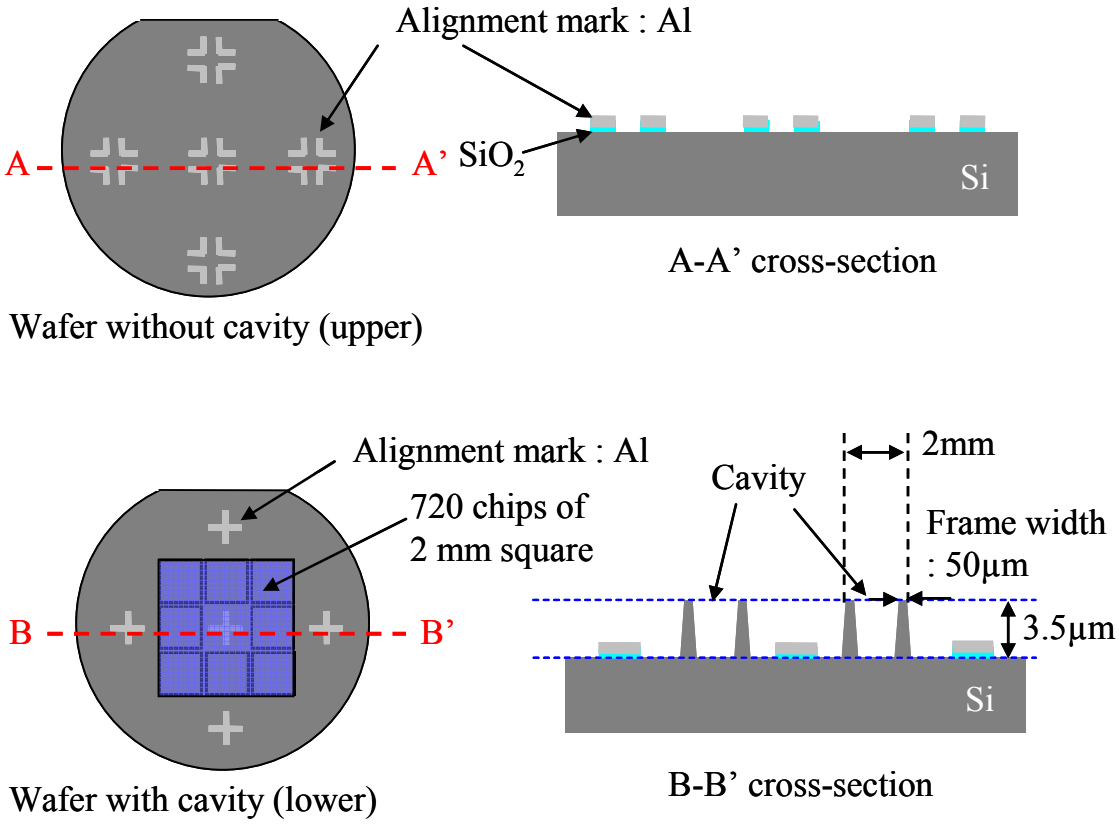
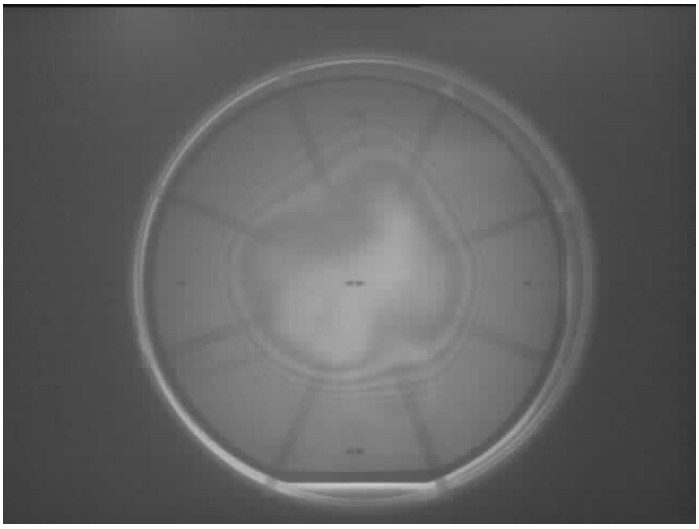


Fig.4.4 Test element group for room-temperature bonding.

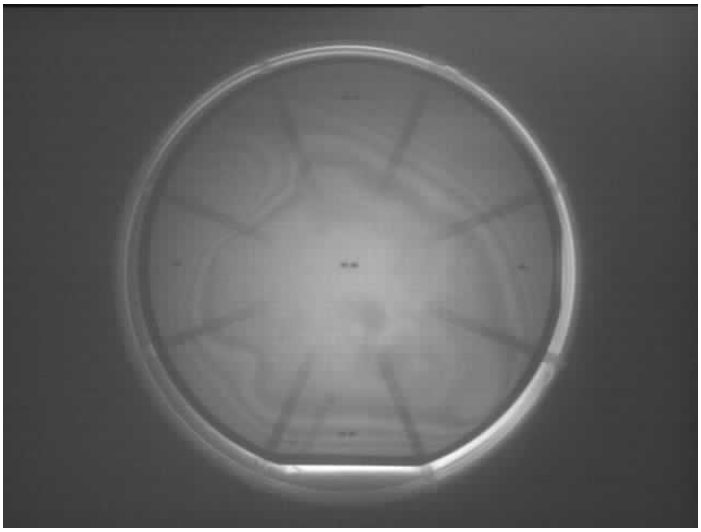
Table 4.1 Conditions for room-temperature bonding.

Vacuum before emission	[Pa]	6.5×10^{-6}
Anode voltage	[V]	100
Anode current	[A]	20
Emission current	[A]	1.15
Keener current	[A]	1.5
Source gas	[sccm]	8.0
HCFS gas	[sccm]	3.0
Emission time	[min.]	6.0
Ion gun height	[mm]	100
Junction load	[N]	20000
Pressure time	[sec]	1200



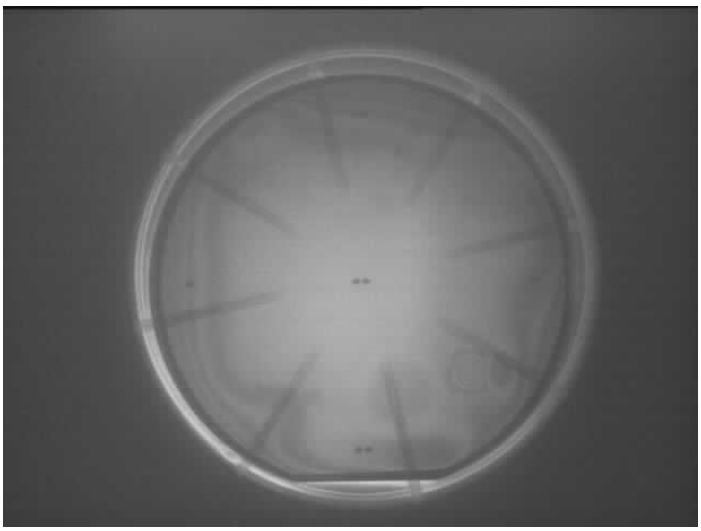
40 kgf

Fig.4.5(a) IR image of Si wafers bonded at room temperature.



200 kgf

Fig.4.5(b) IR image of Si wafers bonded at room temperature.



500 kgf

Fig.4.5(c) IR image of Si wafers bonded at room temperature.

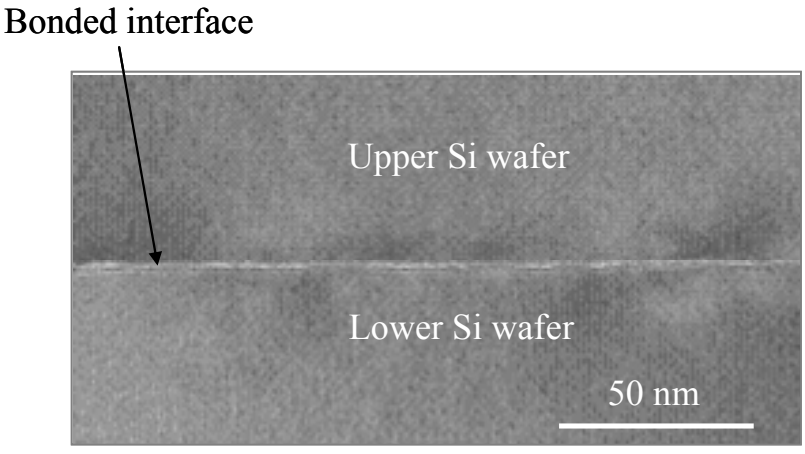


Fig.4.6 TEM photograph of Si wafers bonded interface.

4.3 Hermetic sealing and electric connection

Bonding technologies reported so far are nearly limited to metal-to-metal bonding. In contrast, the room-temperature bonding was studied as a concurrently hermetic sealing and electric connecting bond technology, consisting of forming a silicon dioxide film on the periphery, bonding the facing Si layers to make the cavity in the wafer hermetic, and, at the same time, pressure bonding the facing signal interconnection electrodes to enable conduction [3-5]. Figure 4.7 shows a schematic of bonding method for hermetic sealing and electrical connections. Compared with metal-to-metal bonding, this method is deemed to be stronger as the dangling bonds are activated to become covalent bonds, thus superior long-term reliability is expectable.

The insulation film must fulfill the following conditions at the time of bonding: Ra, average surface roughness of under 1 nm; Rmax, maximum surface roughness of under 10 nm; and the bonding surface needs to be a flat film free of residues. Also, with regards to performing vertical lamination processes, there exists a process to bond IC and MEMS layers. This process requires a flat insulation film for bonding that can be formed at low temperatures in order to reduce thermal damage to the electric interconnections in the IC and MEMS layers. The insulation film has been confirmed that the TEOS silicon dioxide film discussed in Chapter 2 fulfilled the above conditions in terms of both surface roughness and flatness.

Figure 4.8 shows the results of the distribution of TEOS silicon dioxide film thicknesses on a silicon substrate, and Figure 4.9 shows the results of atomic force microscopy (AFM) measurement of TEOS silicon dioxide film surface roughness. It was confirmed that the deviation in the thickness of the TEOS silicon dioxide film was enough level of less than 10 nm, as the result of the measurement, Ra of under 0.2nm and Rmax of under 5nm were obtained.

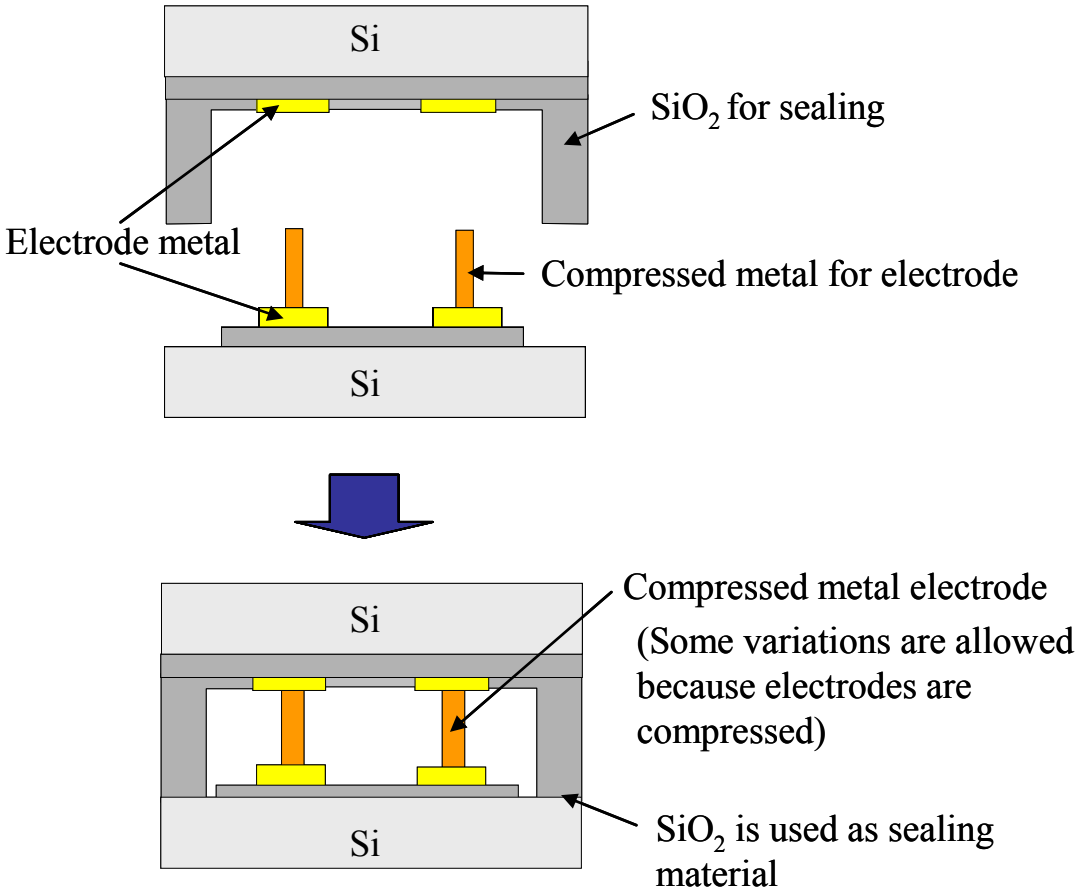


Fig.4.7 Schematic illustrations of concurrent bonding method for hermetic sealing and electric connections.

Plasma TEOS SiO_2 thickness [nm]		
Measurement Point	No.1	No.2
Center	310.2	312.8
Upper	304.0	305.7
Left	312.9	314.8
Lower	311.8	315.0
Rigtht	315.0	316.5
Average	310.8	313.0

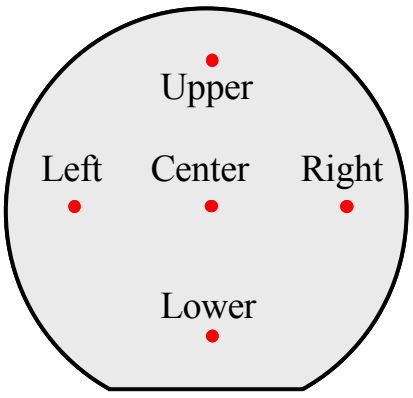
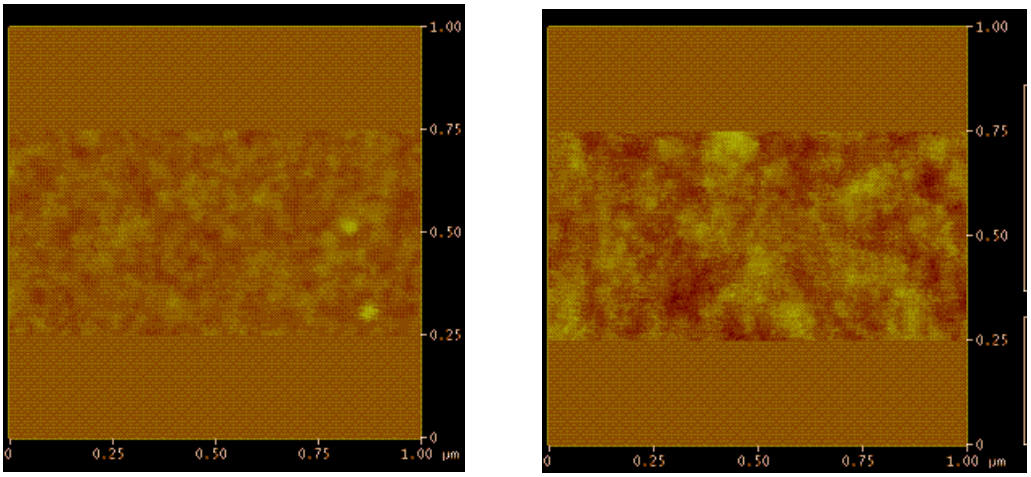


Fig.4.8 Distribution of TEOS silicon dioxide film thicknesses.



(a) Center
- Rmax = 3.97nm
- Ra = 0.19nm
- Thickness = 310nm

(b) Right
- Rmax = 3.69nm
- Ra = 0.18nm
- Thickness = 310nm

Fig.4.9 Results of measuring TEOS silicon dioxide film surface roughness with AFM.

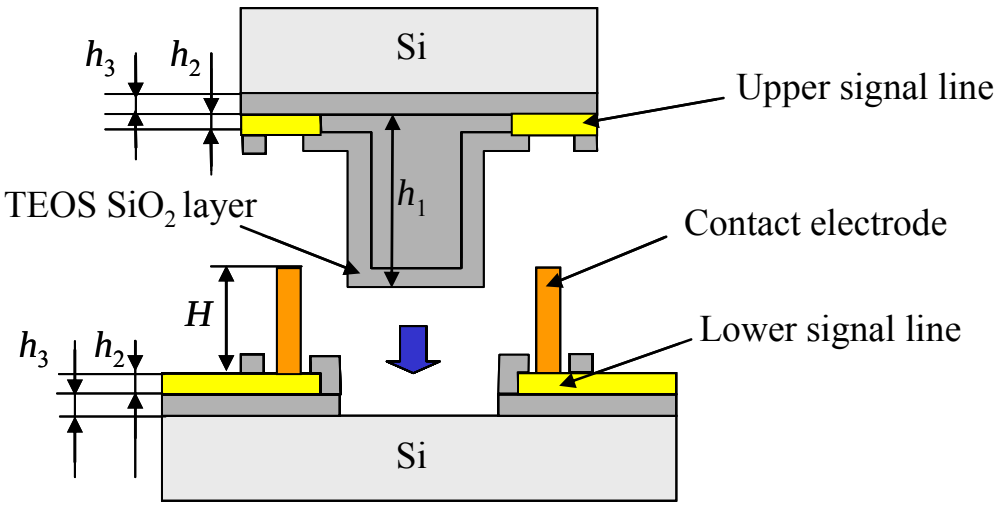
To achieve concurrent bonding, the conducting contact electrodes must be sufficiently pressed and crushed before contact between the TEOS silicon dioxide film formed Si substrate and the Si substrate. However, if the electrodes area is too large or the electrode material is too hard, the interconnections will not crush satisfactorily and sufficient contact will not be realized. Therefore, the design of the Au contact electrode height, area, hardness, and structure is of primary importance. Figure 4.10 shows a schematic of substrate-electrode bonding structure.

Considering the height variation of ±5% while Au deposition was formed by physical vapor deposition (PVD). It is necessary for the height H of Au contact electrodes to be designed according to the following inequality (1). Height control of Au contact electrodes becomes a rule factor of electrical

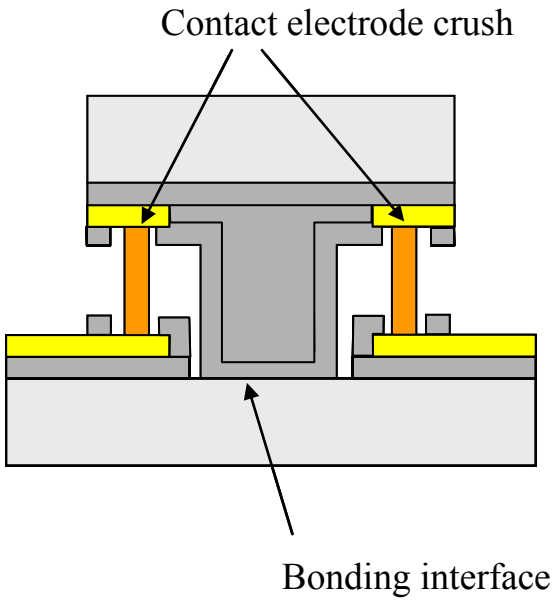
contact and sealing. h_1 is the thickness of TEOS silicon dioxide film, h_2 is the thickness of Cr/Au base electrodes, and h_3 is the thickness of insulator. The height h_1 must be lower than total h_2, h_3, and H height, however, must be higher than the total height considering the amount of compression. In addition, the inequality (1) includes the height variation of $\pm 5\%$, while a Au contact electrodes were formed by deposition. As a result, total height of Au contact electrodes and Cr/Au base electrodes were designed 300 nm higher than sealing height.

$$\frac{h_1 - 1.9h_2 - h_3}{0.950} < H < \frac{h_1 - 2.1h_2 - h_3}{0.785} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

The mechanical characteristic of microfabricated metal pattern is often different from the bulk one. The compressibility of Au contact electrode is also different from bulk one, the compressibility verification was therefore demonstrated, and the result is shown in Figure 4.11.



(a) Structure of substrate bonding surface and electrode.



(b) TEOS SiO_2 layer and Si substrate are bonded after electrodes are crushed.

Fig.4.10 Substrate-electrode bonding region structure.

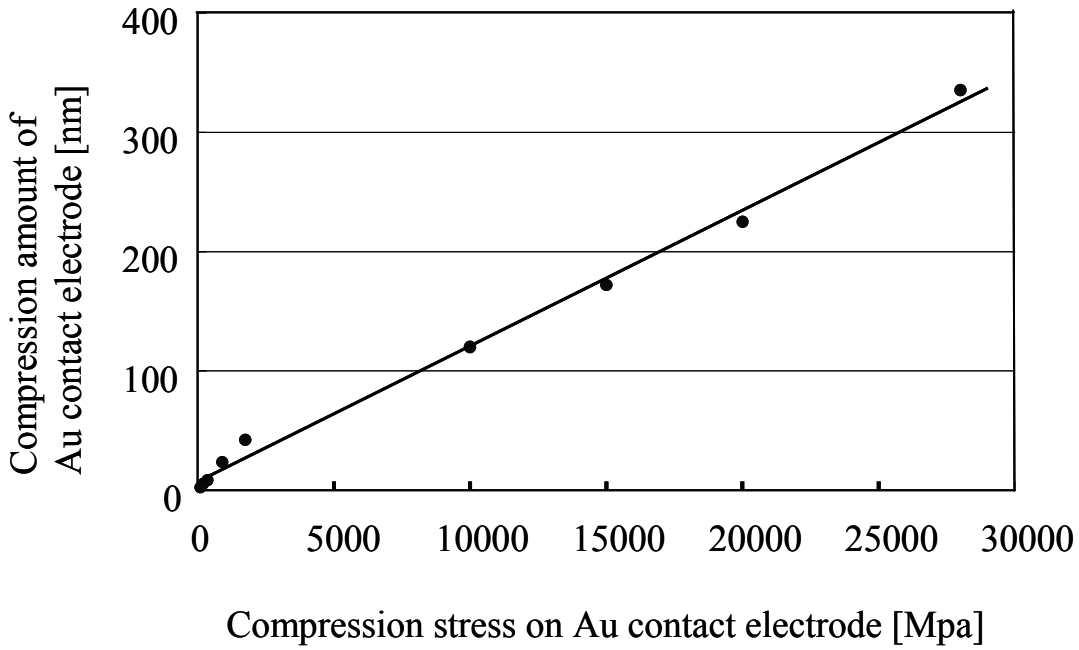
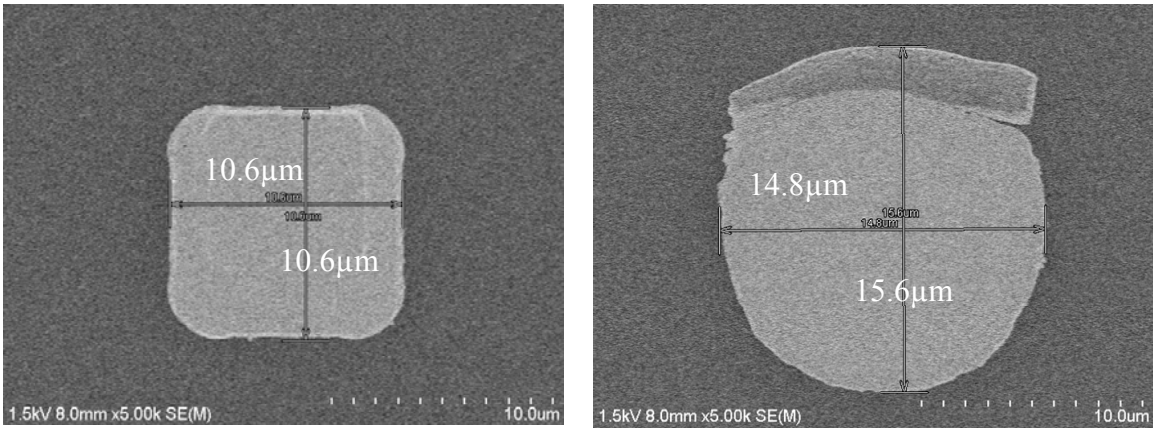


Fig. 4.11 Compressibility verification of microfabricated Au contact electrode.

The correlation between the electrode area and the crush amount was verified when a maximum bonding load of 25,000 MPa was applied and was confirmed that a 10-μm square, a 1-μm height contact electrode was sufficiently crushed to 0.3 μm when the above load was applied to the square area (Table 4.2 and Figure 4.12). Au compressive plastic deformation was expected to be utilized for electrical connection.

Table 4.2 Au bonding electrode crush amounts.

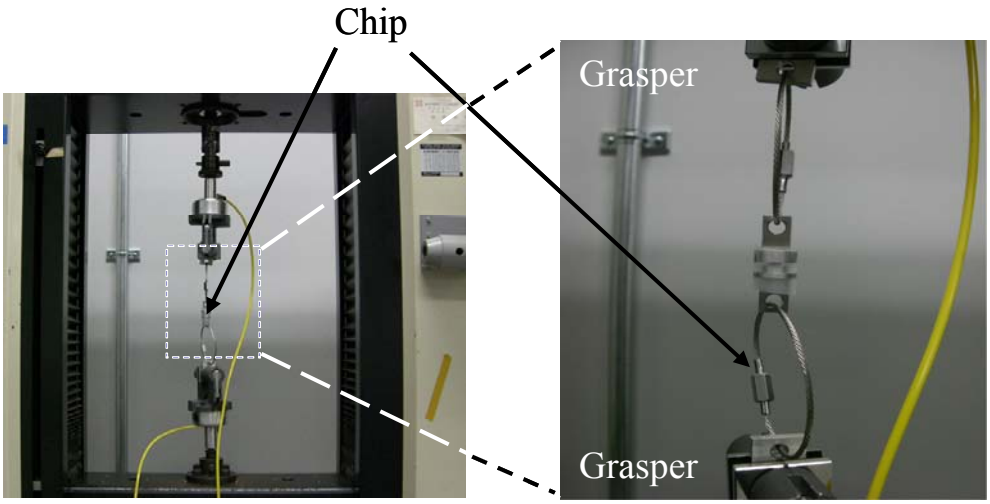
Location No.		1	2	3	4	5	Average	Crush length
Center	[nm]	735.2	648.5	755.6	631.7	714.8	697.2	348.7
Upper	[nm]	511.4	640.8	520.4	746.8	724.7	628.8	409.6
Left	[nm]	723.3	768.1	753.0	789.1	697.4	746.2	290.8
Lower	[nm]	755.4	747.3	764.1	636.2	715.4	723.7	314.3
Right	[nm]	720.4	710.1	778.7	659.9	756.1	725.0	313.3
Average	[nm]	689.1	703.0	714.4	692.7	721.7	704.2	335.3



Before pressurizing After pressurizing

Fig.4.12 SEM photographs of Au bonding electrode before and after pressurization.

The bonding strength was measured using the chips obtained by dicing the wafer. To evaluate the bonding strength, tensile strength tests were conducted by tensile strength testing machine as shown in Figure 4.13. These tests demonstrated that the bonding strength had a bond binding energy of 0.8 to 1.1 J/mm^2. This value is more than enough to maintain the bonding and therefore able to withstand practical use.



(a) External view of tensile strength testing machine

(b) Test sample after tensile strength test

Fig.4.13 Photographs of tensile strength testing machine and test sample after tensile strength test.

The test wafer shown in Figure 4.14 was fabricated, and the post-bonding resistance was also assessed, by bonding wafers with patterns including two Au contact electrodes placed wafers with the Au planar interconnection electrode, by measuring the resistance after the wafers were bonded, and the contact resistance at the bonding interface was assessed by using a four probe terminal resistance measurement method. Figure 4.14 is a schematic illustration of this resistance measurement and Figure 4.15 depicts a scene from actual post-bonding resistance measurement.

Table 4.3 shows calculation and measurement values of resistance after bonding.

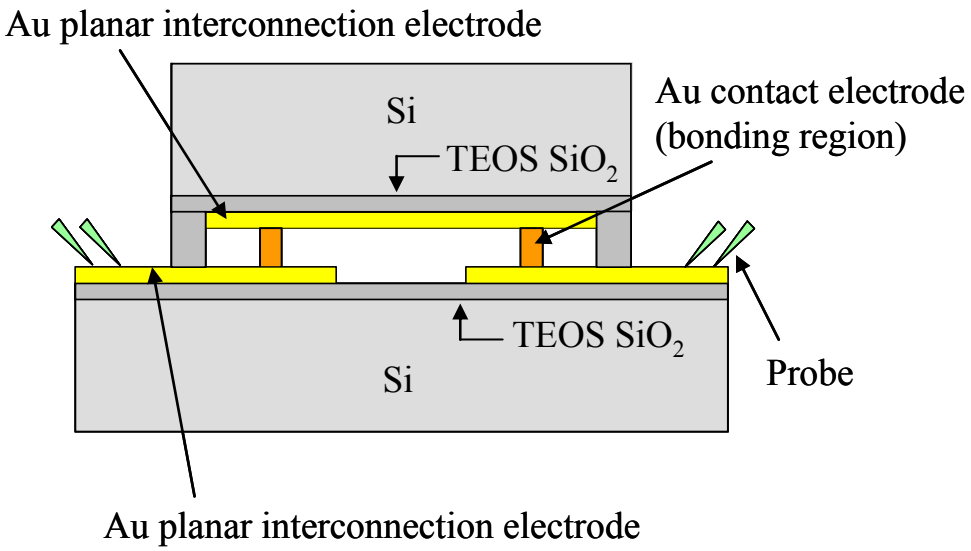


Fig.4.14 Schematic illustration of post-bonding resistance measurement; The post-bonding resistance was measured by bonding wafers with patterns including two Au contact electrodes placed between wafers with the Au planar interconnection electrodes, and the contact resistance at the bonding interface was measured by using a four probe terminal resistance measurement method.

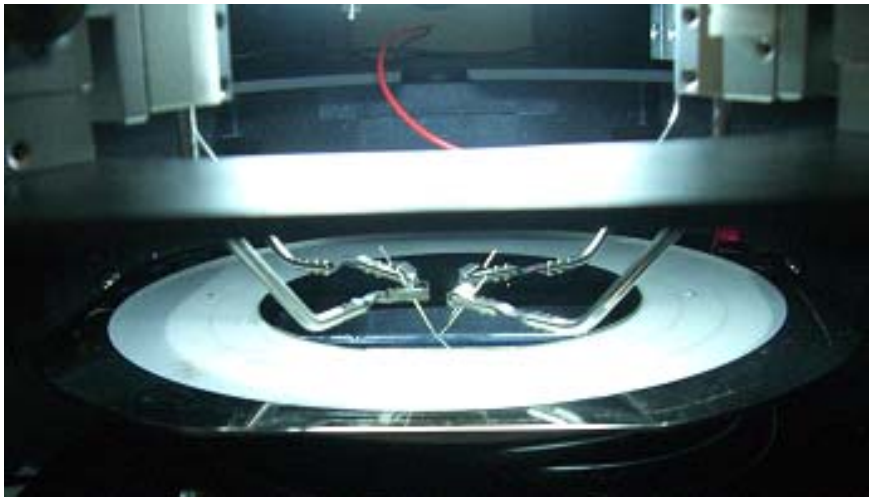


Fig.4.15 Photograph of scene from actual post-bonding resistance measurement by four probe terminal resistance measurement method.

Table 4.3 Post-bonding resistance measurements.

Property Dimension		Value
Au resistivity	[Ωm]	2.35×10^{-8}
Interconnect length	[μm]	2255
Interconnect width	[μm]	150
Interconnect thickness	[μm]	0.3
Bond thickness	[μm]	0.6
Bond area	[μm^2]	100
Calculated resistance	[Ω]	1.18
Measured resistance	[Ω]	9.44

The difference between the calculated and measured resistance values seems to be caused by the contact resistance at the bonding interface between

the compressed electrode metal and the electrode metal, as well as the geometric properties and cleanness of the metal surface.

The measured resistance value after bonding as shown in Figure 4.14 was 9.44 ohms in contrast to the calculated resistance value of 1.18 ohms calculated from the length, thickness, and resistivity of the planer interconnection and the contact electrode. Because the pre-bonding interconnection resistance value was almost equal to the calculated value, the contact resistance at the interface seems to be the major cause of increased interconnection resistance.

The surface was likely contaminated with organic substances during the resist removal process. A cleaning step was therefore added using N-Methyl-2-Pyrrolidone (NMP). Table 4.4 shows the results of measuring resistances after changing the cleaning process.

As a result, a post-bonding resistance of 3.17 ohms was obtained. Although this value is still higher than the calculated value, it has been revealed that by taking into account organic contaminants at the bonding interface, the contact resistance could be reduced.

Table 4.4 Results of measuring resistances after changing the cleaning process.

Property Dimension		Value
Au resistivity	[Ωm]	2.35×10^{-8}
Interconnect length	[μm]	2255
Interconnect width	[μm]	150
Interconnect thickness	[μm]	0.3
Bond thickness	[μm]	0.6
Bond area	[μm^2]	100
Calculated resistance	[Ω]	1.18
Measured resistance	[Ω]	3.17

Finally, bonding alignment accuracy was evaluated. When 5-μm diameter through-holes are used as signal interconnections, it can easily be expected that adequate conduction will not be achieved through poor bonding alignment accuracy. Ultimately, technology that can always realize ±1-μm alignment accuracy is required. To achieve above alignment accuracy, a high-accuracy alignment method based on the "vernier caliper pattern" was used. The vernier calipers patterns sets up referred secondary scale in parallel in main scale by -0.2 μm pitch, and a longest line at the center is observed as straight line when there is no alignment error. For example, when 0.4 μm shifts, it is observed as straight line as the 2nd main scale and secondary scale overlap with sufficient accuracy from a longest line, and a highly-accurate alignment becomes possible. As shown in Figure 4.16, alignment errors were measured by using a high-precision IR microscope and Figure 4.17 shows the results of two test post-bonding wafers which were confirmed a high accuracy of ±2 μm in both the X and Y directions. Using this technology, the method was improved and finally was achieved a high accuracy of ±1 μm as described in the next section.

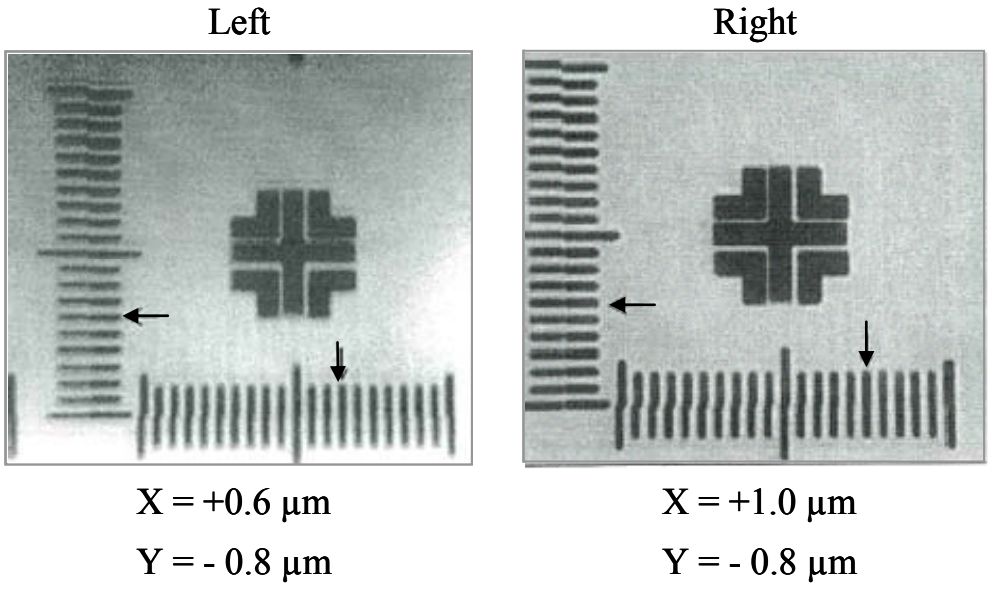


Fig.4.16 Post-bonding alignment errors. (IR microscope photograph)

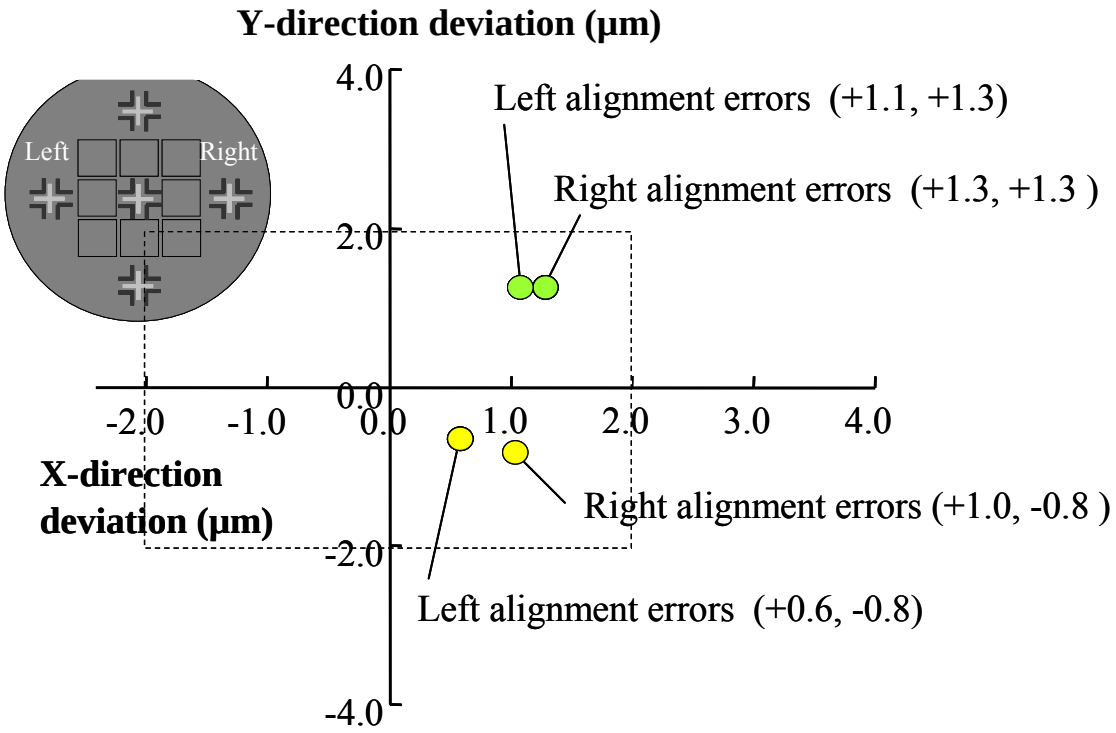


Fig.4.17 Alignment error measurement results of two sets of post-bonding wafers; Alignment errors in both the X and Y directions were confirmed a high accuracy within ±2 μm.

4.4 Multi-layer vertical integration bonding

Although the main theme of this study is MEMS-MEMS bonding, which includes the bonding in infrared array sensors and micromirror arrays, as stated in the "Introduction" bonding of MEMS sensor wafers, which include the formation of through-hole interconnections, and IC wafers, which process signals, is also an important study theme that will extend to a wider field of applications. As a result, the bonding of IC wafers and MEMS wafers was also studied.

Issues concerning IC-MEMS bonding are the surface geometry and surface material of the IC wafer. Normally, as IC wafers are formed by lamination processes, they have some localized thicker places than other

places around the electrodes as shown in figure 4.18. As a consequence, the bonding surface must be formed higher than the film surface in this localized thick area. In addition, AlSi is generally used as the electrode material for IC, but is not suitable for bonding electrodes. Furthermore, SiN, which is used in a moisture-proof film formed on the IC, cannot be bonded easily at room temperature.

Therefore, a thick TEOS silicon dioxide film was formed as a bonding film on the surface of IC and flattened and smoothed the surface by applying CMP. The surface roughness after CMP was expressed by the conditions: Ra < 1 nm and Rmax < 10 nm, indicating that it adequately fulfilled the bonding conditions.

In addition, Au contact electrodes on the lead-out electrodes ware formed by using the lift-off method because we were anxious about wet etching, which could damage the IC.

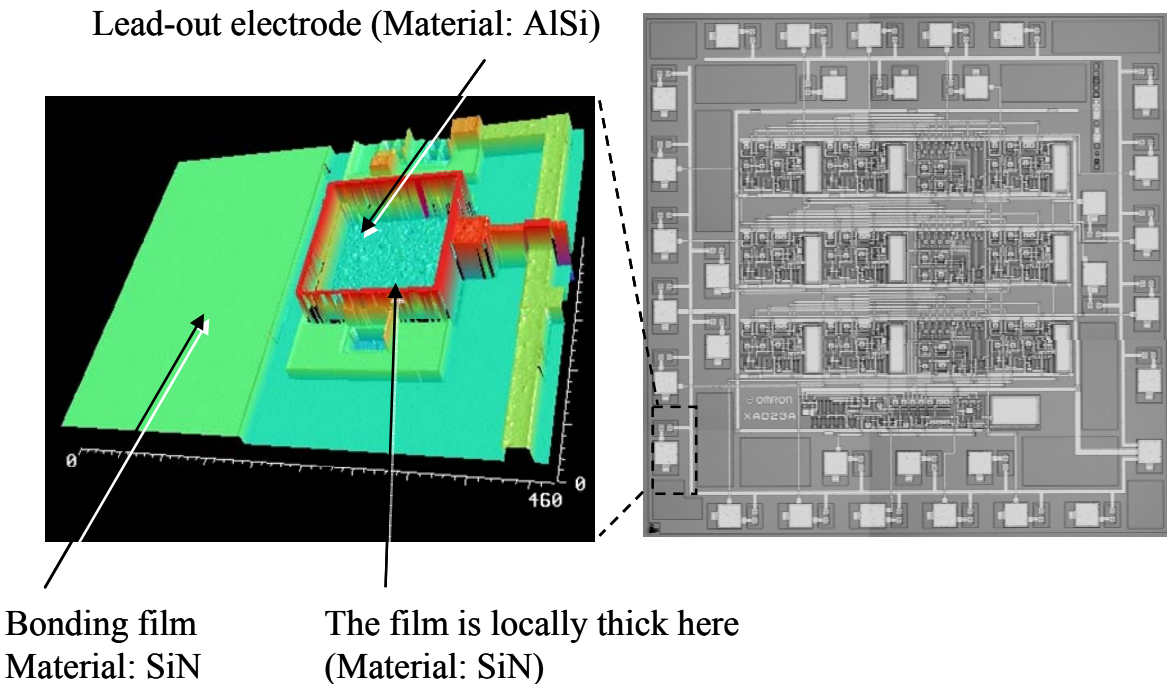
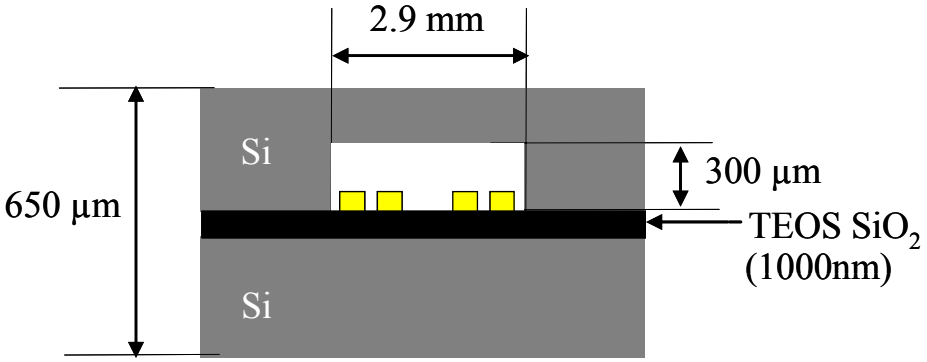


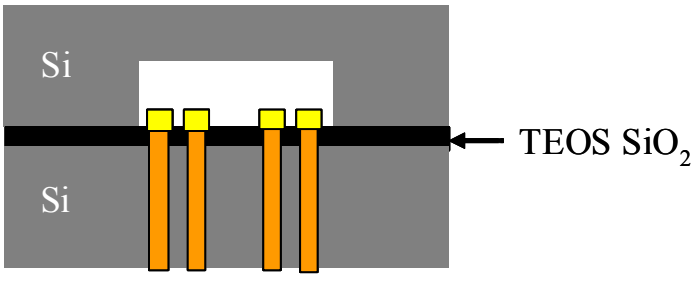
Fig.4.18 Example of IC surface profile. (near an electrode pad)

4.4.1 Verification of hermetic sealing

As already stated in Chapter 1, hermetic sealing is extremely important to increase the sensitivity of infrared sensors. Since there was no research report about the hermetic sealing of through-holes bonded at room temperature, test samples were fabricated for confirmation. The probable leak paths include Si-SiO_2 bonding interfaces and though-hole interconnections. Control samples were also fabricated having no through-hole interconnections for comparison as shown in Figure 4.19 and conducted similar leak tests on these samples [6].



(a) Si-SiO2 bonding sample.



(b) Si-SiO2 with through-hole interconnections sample. (Cu electrodes)

Fig.4.19 Cross-sectional image of sample with hermetic sealing.

It should also be noted that the wafer with through-hole interconnections was once exposed to a temperature of nearly 100°C when the Au electrodes were formed.

Bonded samples were diced into chips, were checked for poor bonding using an infrared confocal microscope (LEXT-IR manufactured by Olympus), and then helium (He) leakage tests was conducted on 30 chips. Within the vacuum chamber, bonded samples were evaluated, after pressurizing helium gas with 0.42 kg/cm^2 pressure for 2 hours. The detection limit of these He leakage tests was 5 x 10^{-9} Pa•m^3/s. Figure 4.20 shows He leakage test results presented in the compliant of the MIL Standard (MIL-STD-883E). The tests demonstrated that the leakage from all 30 chips tested was less than the detection limitation and Si-SiO_2 bonding proved to have enough a hermetic sealing that stands for practical use.

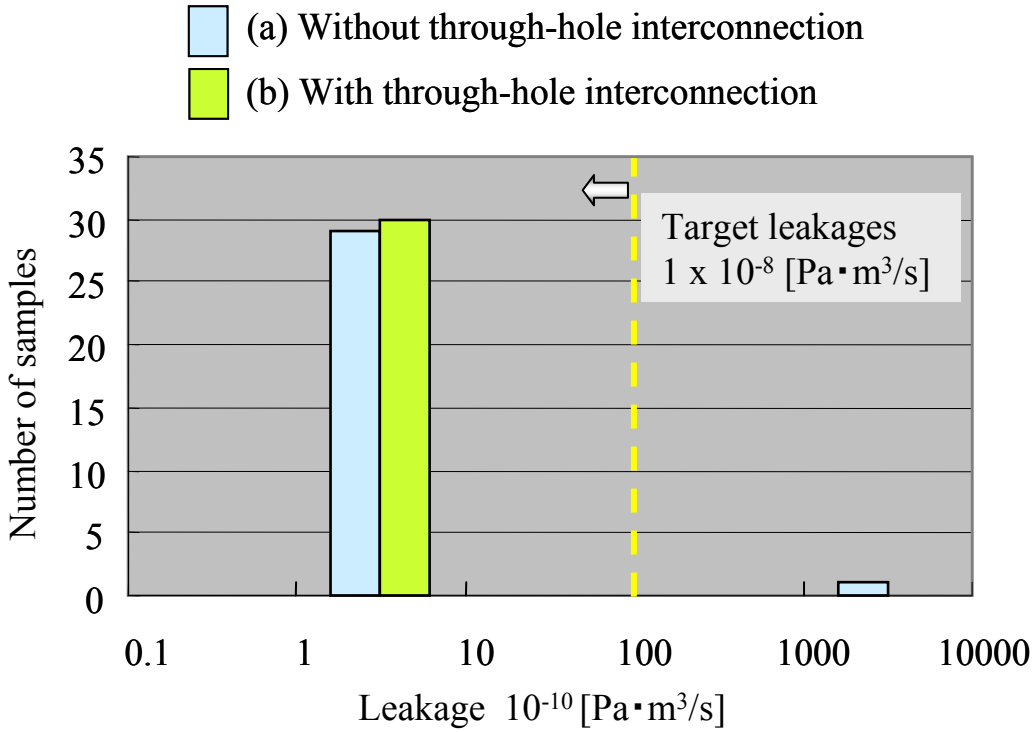


Fig.4.20 Helium leakage test results presented in the compliant of MIL Standard.

4.4.2 Verification of electric resistance and alignment accuracy

When 5-μm diameter through-holes are used as signal interconnections, it can easily be expected that adequate conduction will not be achieved through poor bonding alignment accuracy. Therefore it is necessary to confirm there is alignment accuracy of ±1 μm.

It was achieved that a stable alignment accuracy of ±1 μm or less even on single-side polished wafers by implementing alignment feature improvements, including studying of vernier caliper patterns for high-accuracy bonding, use of a high-resolution IR microscope and a stage providing a resolution of 100 nm. Figure 4.21 shows IR microscope photographs of two-layer bonding (MEMS-MEMS) alignment errors, whereas Figure 4.22 shows IR microscope photographs of three-layer bonding (IC-MEMS-MEMS) alignment errors. In Figure 4.22, although the alignment of an IC wafer and a MEMS wafer is shown, the IR microscope photographs are indistinct, because transmitted infrared rays scattered and reflected by lower MEMS wafer.

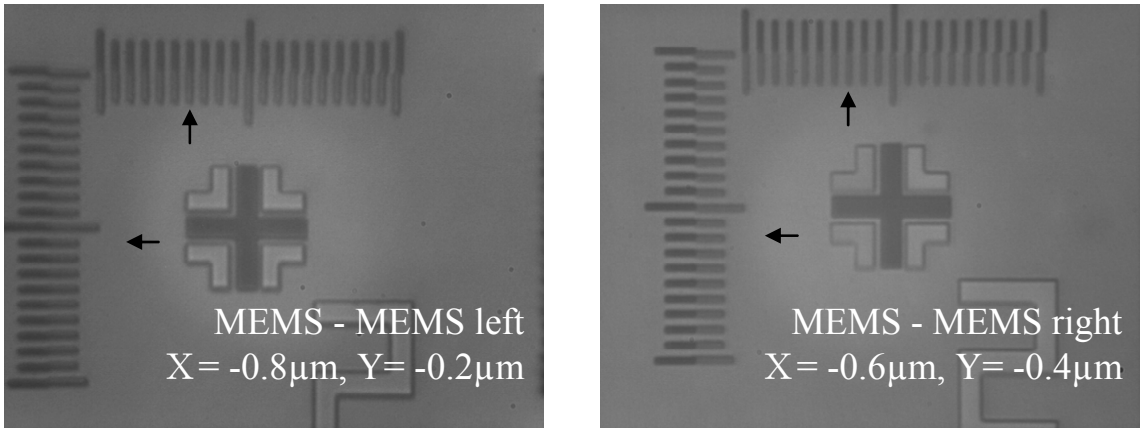


Fig.4.21 IR microscope photographs of two-layer bonding (MEMS-MEMS).

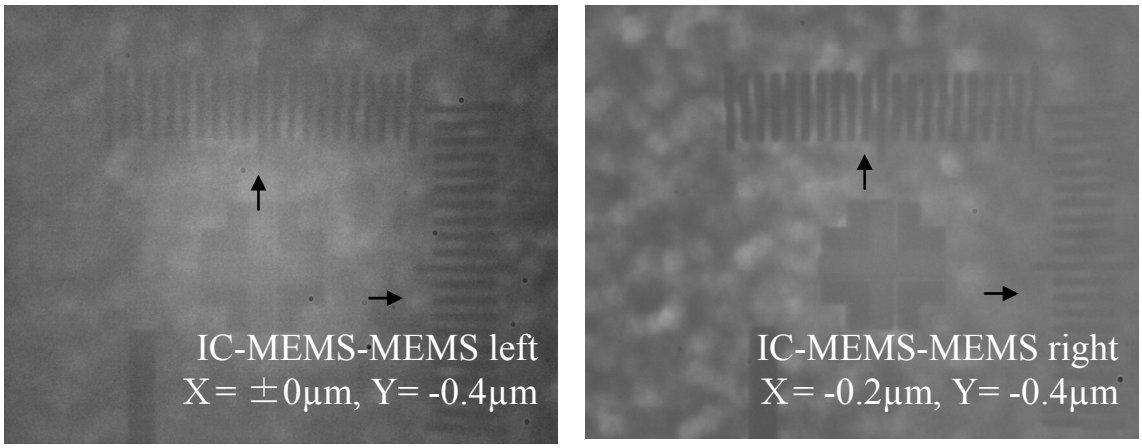
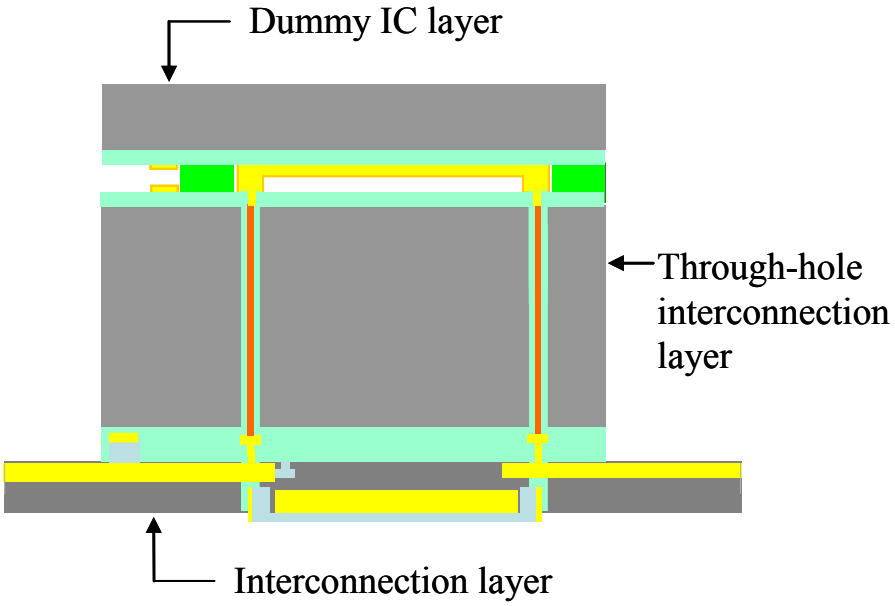


Fig.4.22 IR microscope photographs of three-layer bonding (IC-MEMS-MEMS).

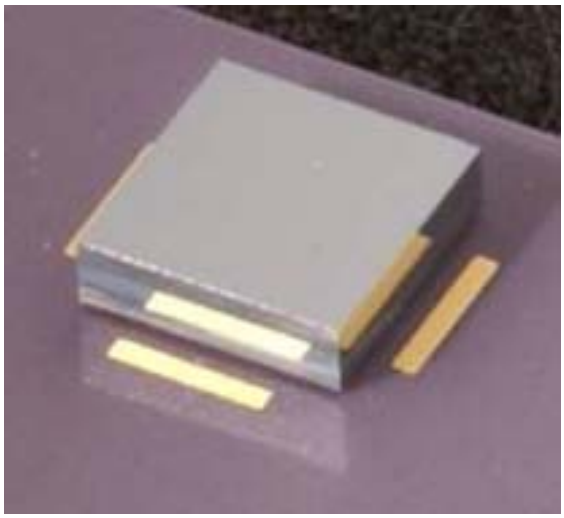
4.5 Results and Discussion

By integrating through-hole formation technology, through-hole interconnection formation technology, and wafer-level bonding technology, wafer was bonded as between IC substrates and MEMS-compatible substrates with through-hole interconnections, and bottom interconnection layers. Then the resistance was measured in the interconnection section via two through-hole interconnections and four bonds and was assessed its characteristics. Figure 4.23 shows a schematic illustration and microscope photograph of the three-layer bonding model. Figure 4.24 shows the three-layer model fabrication process and Figure 4.25 shows cross-sectional views of the three-layer bonding model. Also bond strength assessment tests were conducted, which were similar to tests conducted to assess the wafer-level bonding technology and confirmed that the bond strength was 0.9 to 1.1 J/mm^2 in terms of binding energy, which is almost equal to wafer-level bonding strength. It was expected that three-layer bonding would be less strong than two-layer bonding because the former was more susceptible to

wafer warpage, deformation, and hardness. However, the strengths of three-layer bonding and two-layer bonding were comparable.



(a) Schematic illustration



(b) Microscope photograph

Fig.4.23 Schematic illustration of three-layer bonding model and microscope photograph.

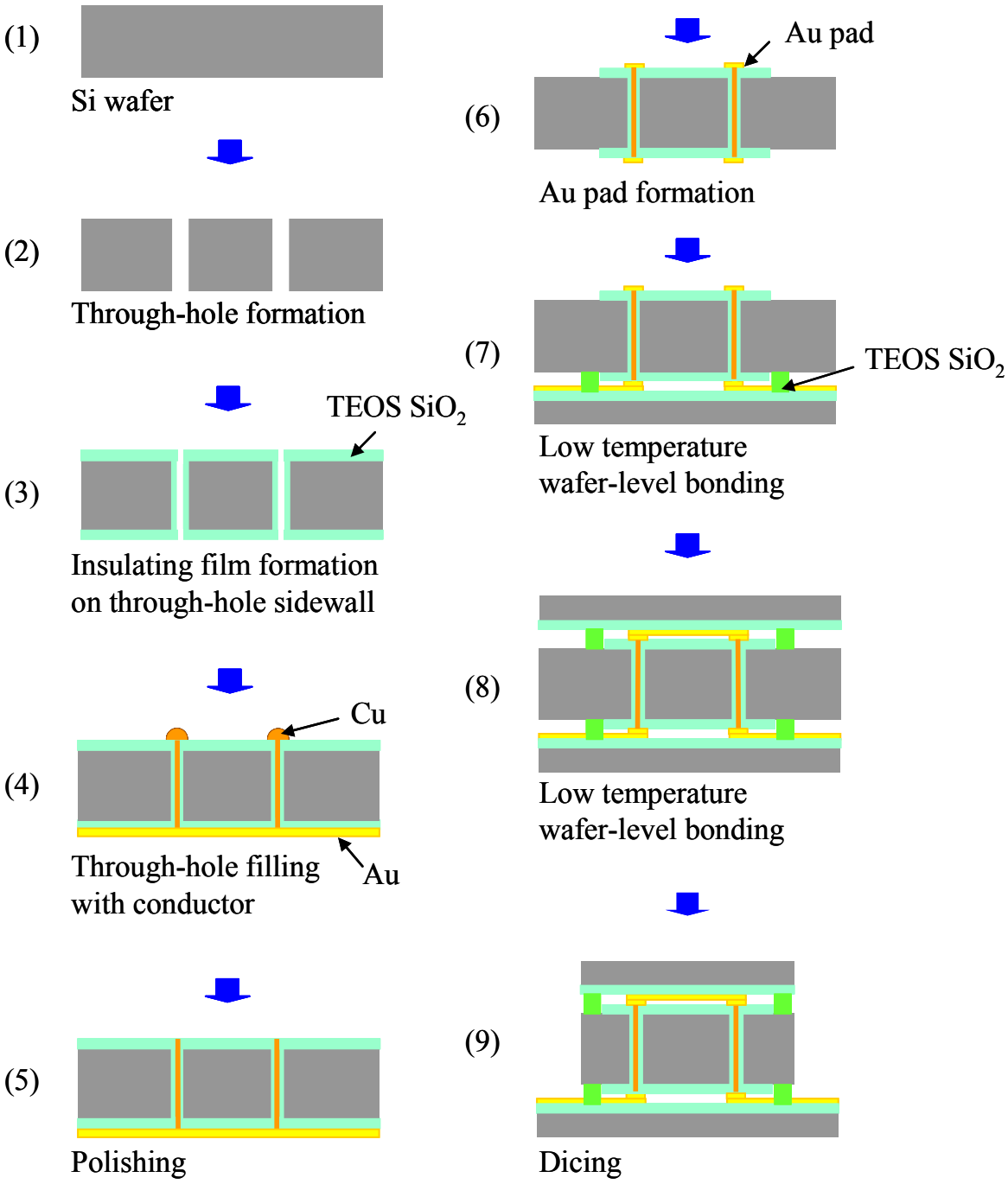


Fig.4.24 Schematic of three-layer model processing.

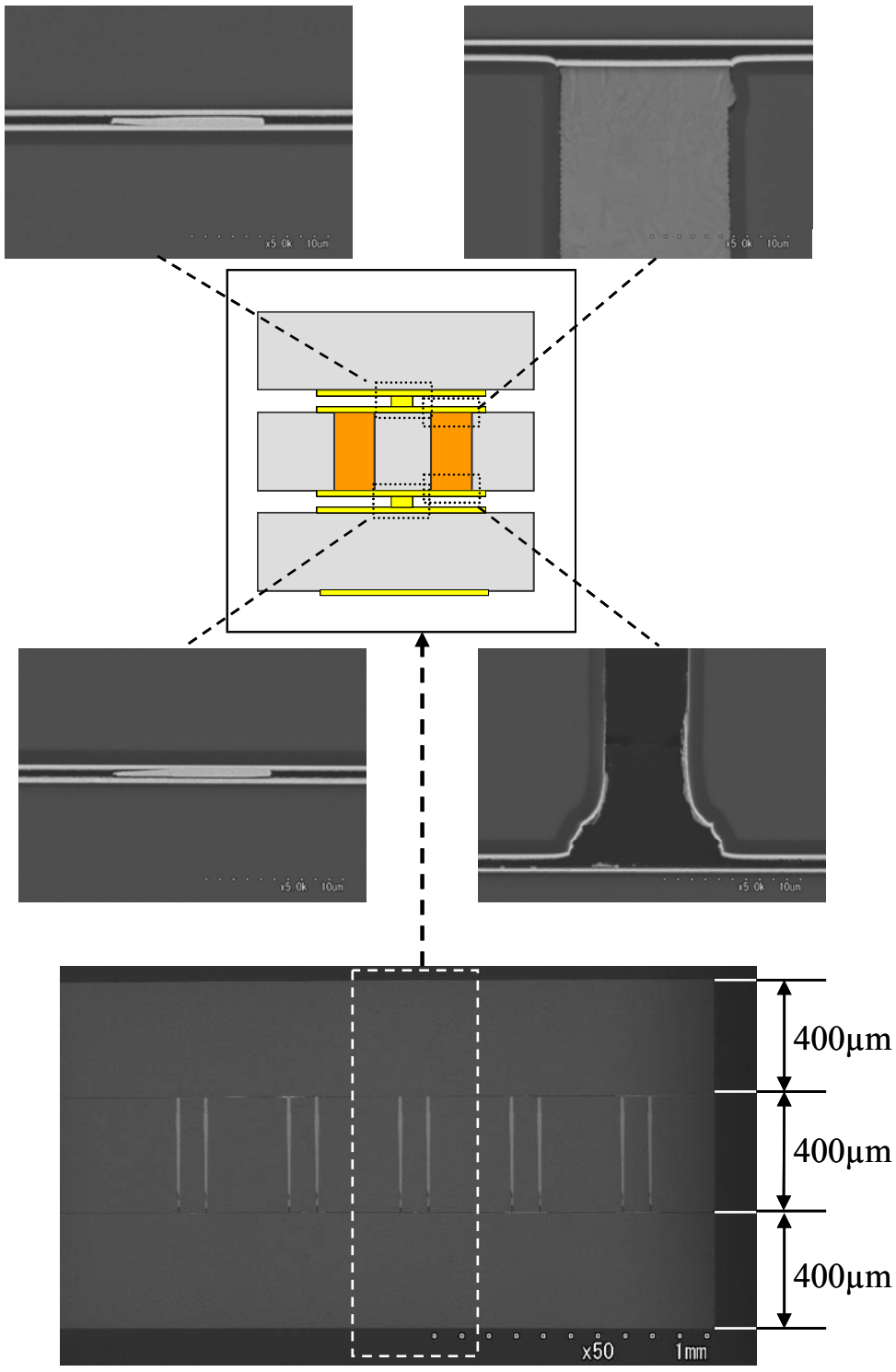


Fig.4.25 Cross-sectional view of three-layer bonding model. (Diagram and SEM photographs)

Then a three-layer laminated structure consisting of an IC wafer layer was fabricated, a MEMS-structured wafer layer with through-hole interconnections, and a laminated wafer layer containing only planer interconnection electrodes, in this order from top to bottom. Figure 4.26 shows a schematic illustration of this three-layer bonding model including an MEMS layer having a bridge structure, and Figure 4.27 shows a cross-sectional SEM photograph. The diameter and aspect ratio of each through-hole interconnection was 5-μm diameter and 50:1, respectively. Electric conduction was provided from the pads on the back of the third layer, via the through-hole interconnections, to the ICs in the first layer. It is possible to laminate wafers containing an MEMS structure, which is typically pyramidal, without damaging the MEMS structure.

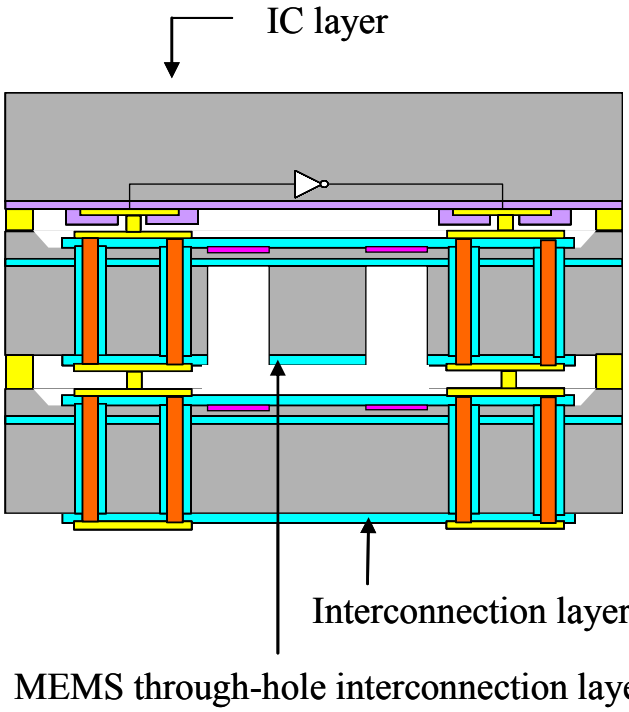
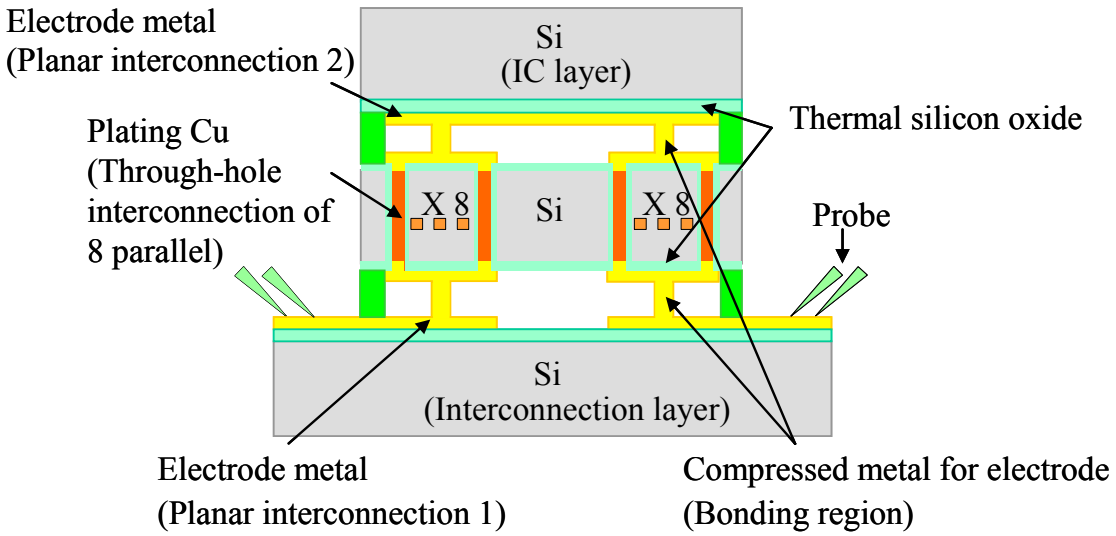


Fig.4.26 Schematic illustration of three-layer bonding model including an MEMS layer.

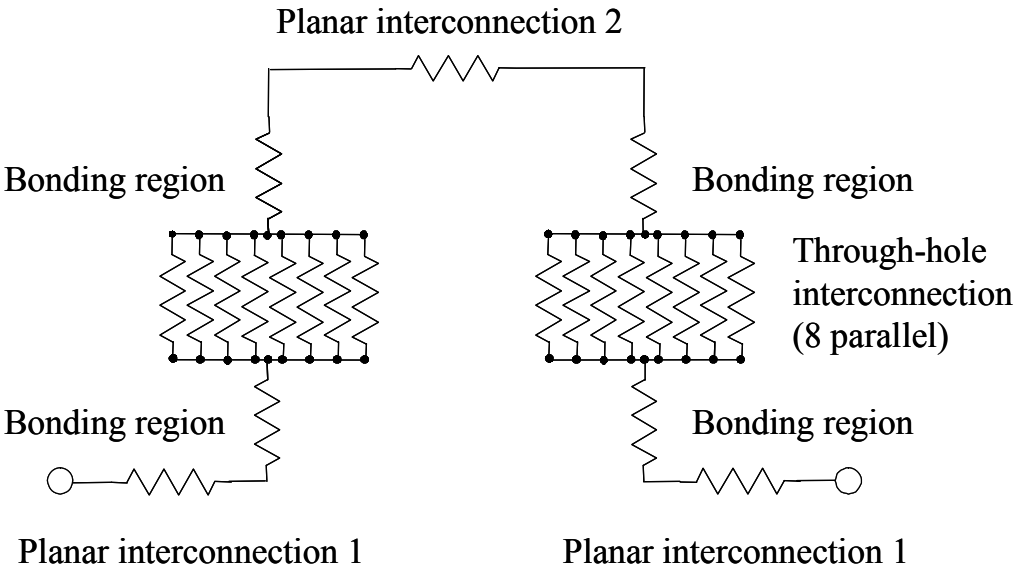
Fig.4.27 Cross-sectional view of three bonded layers including an MEMS layer having a bridge structure; MEMS layer is a piezoresistive 3-axis accelerometer.

To perform an overall electrical assessment of through-hole interconnections bonded to wafers, a sample was fabricated by bonding two planar interconnection-only wafer layers and one wafer layer containing through-hole interconnections, forming the circuit shown in Figure 4.28(b). Figure 4.28(a) shows schematic illustration of the wafers as bonded. The resistance of the interconnections including through-hole interconnections and wafer bonds was measured and table 4.5 shows the measurement results.

The measurement result of 37.6 ohms was found to be 17.9 ohms higher than the calculated resistance of 18.7 ohms previously measured from the through-hole interconnection resistance value, the planar interconnection resistance and the wafer bond resistance. This higher resistance seems to be caused by the additional contact resistance at the bond. However, this level of increase will raise no problem in its application to infrared MEMS array sensors. However, if improvement is required, modification of the surface conditions could reduce resistance further.



(a) Schematic illustration.



(b) Circuit diagram.

Fig.4.28 Schematic illustration of three-layer bonding resistance measuring system and equivalent circuit.

Table 4.5 Three-layer bonding resistance measurement results.

Property Dimension		Value
Au resistivity	[Ωm]	$2.23x10^{-8}$
Cu resistivity	[Ωm]	$1.67x10^{-8}$
TSV length	[μm]	400
TSV diameter	[μm]	6.8
Planar 1 line length	[μm]	1850
Planar 1 line width	[μm]	150
Planar 2 line length	[μm]	250
Planar 2 line width	[μm]	50
Planar line thickness	[μm]	0.3
Bond thickness	[μm]	0.6
Bond area	[$μm^2$]	100
Planar line resistance	[Ω]	1.36
Contact resistance	[Ω]	4.13
TSV resistance	[Ω]	3.36
Calculated combined resistance	[Ω]	18.7
Measured combined resistance	[Ω]	37.6

Further, lead-out electrodes were added on the back of the bottom layer of the sample shown in Figure 4.27, passed a current through the through-hole interconnections in the bottom and middle layers, and measured the resistance of the ICs in the top layer. The result of this measurement demonstrated that the resistance change from the pre-bonding condition to the post-bonding three-layer laminated condition was from 36.4 to 37.9 kilo-ohms, a difference raising no problem with operations.

Under the development of through-hole formation, interconnection formation and bonding technologies, MEMS-MEMS-IC were layered and through the development of bonding technologies which allow electrical connections have established vertical lamination MEMS technology.

4.6 Conclusion

This chapter has described the establishment of a room-temperature bonding technology based on the surface activation method using ion gun bombardment that will not produce adverse thermal effects on MEMS wafers and IC wafers. It was confirmed that an alignment accuracy of ±1μm is sufficient for 5-μm-diameter micro through-hole interconnections using three-layer wafers as described in Chapter 3. New sealing technology was also developed to realize concurrent bonding for hermetic sealing and electric connections. Helium leakage test conforming to the MIL Standard (MIL-STD-883E) demonstrated that the hermetic sealing of the through-hole interconnection was such that the leakage was within the detection limit. In addition the resistance of the post-bonding electric connection was achieved sufficiently low for actual application. It can thus be concluded that high-precision room-temperature wafer level bonding technology that will be useful for infrared MEMS array sensor is now available.

References

[1] M.Moriguchi, M.Shiozaki, S.Sasaki, and M.Oba, ECS Trans. Vol.16, Issue 8, **125**, 2008

[2] M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, IEEJ Trans. Sensors and Micromechanics, Vol.130, No.5, **152**, 2010

[3] M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, ECS Trans. Vol.16, Issue 8, **57**, 2008

[4] M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, Electrochemical and Solid-state Science (PRiME), **2168**, 2008

[5] M.Moriguchi, M.Shiozaki, S.Sasaki, and M.Oba, Electrochemical and Solid-state Science (PRiME), **2180**, 2008

[6] Y.Koyama, M.Ohira, M.Shiozaki, S.Sasaki, and M.Oba, Proc. the 26th Symposium on Sensors, Micromachines & Applied Systems, **554**, 2009

Summary

As part of efforts from an energy saving standpoint by further achieving miniaturization and sensitivity enhancement of infrared sensors, used for the detection of people, in home electric appliances such as air conditioners and Flat-Panel TVs, this thesis discussed a technology that vertically integrates infrared sensor arrays and micromirror arrays in wafers containing 5-μm-diameter through-hole interconnections.

Chapter 1 proposed a new structure that allows the following methods to be implemented at the chip level for high-sensitive infrared MEMS array sensor: (a) a method for concentrating infrared rays using an arrangement where sensors face micromirrors on a one-to-one basis to increase the sensitivity of thermopile sensors, which are compatible with semiconductor processes, and (b) a method for increasing the thermal insulation to increase the hot junction temperature of the thermopile. Infrared sensors and micromirrors were fabricated and the results verified.

The infrared sensor was arranged in a 16 x 16 array, with a size of 150 μm x 150 μm each. Each thermopile, created from connecting p-type Si interconnections and n-type Si interconnections was formed on an insulation film of membrane structure, formed by anisotropic wet etching atop the surface of a Si wafer and used as a temperature sensor.

Micromirrors were fabricated by forming undulations on an Si substrate using the lag effect of DRIE, flattening the side walls through isotropic etching, and forming a reflective surface by vapor-depositing gold. The necessary design and process parameters were extracted, including the relationship between the opening area and the etching depth determined through experimentation with the resulting cross-sectional shapes and focal distance of 145 μm proved to be nearly as expected from the design.

The infrared sensor array and micromirror array were bonded face-to-face at chip level and mounted on a TO-8 size metal stem and the effect of infrared

ray sensitivity was measured upon exposure to a blackbody furnace. A 1.3-time concentration effect by the mirror and a 1.4-time thermal insulation effect under vacuum conditions were obtained. In addition, it was found that a 4-time larger concentration effect, a 7-time larger vacuum's thermal insulation effect and, nearly a 30-time more sensitive infrared sensor in total by narrowing the width of poly-Si interconnection line of the thermopile from 6 μm to 1.5 μm can be obtained.

After verifying the proposed structure has come to the realization that for high-sensitive infrared MEMS array sensor, micromirror wafer containing through-hole interconnections and the method by which infrared sensor array are bonded at the wafer level as discussed in Chapter 2 are important from the viewpoints of miniaturization, high reliability, and low cost.

In Chapter 2, after assumptions that for practical level of use, a through-hole diameter of 5 μm and an aspect ratio of at least 50 be formed in MEMS device wafers for infrared sensor arrays, and discussing the results of individual process for each section, the assumption was of a practical level has been proved. Details of each section are as follows:

First, high-aspect-ratio dry etching technology was discussed, focusing on thick-film resist formation technology and dry etching technology. The resulting technology proved to be successful in forming vertical holes with a diameter of 5 μm and an aspect ratio of 50 in a 250-μm-thick silicon wafer.

Second, the result of a double-side etching method to form through-holes with a 5-μm diameter and 52:1 aspect ratio in SOI wafers, the use of which is extending to MEMS devices, was presented, along with technical view concerning positioning accuracy as the problem to be solved for better through-hole formation by double-side etching on SOI wafers.

This chapter was concluded by the proposal of a PECVD-based oxide film formation technology using O_3-TEOS gas as a method used to form an insulation film. This method proved to be capable of forming a 500-nm-thick uniform oxide film over the through-holes.

Chapter 3 discussed the establishment of two interconnection formation methods: the bottom-up plating method based on the Cu interconnection formation which is applicable to both signal and power interconnections and the LPCVD-based doped poly-Si method, one of the Via-First approaches with good process affinity and is especially effective for signal interconnections.

The bottom-up plating method, for which a seed layer interconnection jig was fabricated to apply a uniform electric field over the wafer surface, succeeded in forming micro through-hole interconnections with a 5-μm diameter and 50:1 aspect ratio thanks to the use of a seed layer consisting of 0.05-μm-thick Cr and 2-μm-thick Au sputtered films. The resulting interconnections proved to be of low resistance comparable to metal film interconnections. In addition, the usefulness of a conductive tape in reducing the time of the seed layer formation process was confirmed. A high-aspect ratio through-hole interconnection formation technology useful for infrared MEMS array sensor was thus established.

Chapter 4 discussed the establishment of a room-temperature bonding technology based on ion-bombardment surface activation that will not produce adverse thermal effect on the MEMS and IC wafers. The alignment accuracy of ±1 μm, which was achieved as discussed in Chapter 3 and considered as sufficient for micro through-hole interconnections with a 5-μm diameter, was also achieved in a three-layer wafer structure. Additionally, technology was developed that realizes the concurrent bonding of electrical connections and of hermetic sealing, which is important for MEMS such as accelerometers, absolute pressure sensors, and high-sensitive infrared sensors. Helium leakage tests conforming to the MIL Standard (MIL-STD-883E) demonstrated that the hermetic sealing of the through-hole interconnection proved to be such that the leakage was within the detection limit.

In addition, it was demonstrated that the resistance of the post-bonding electric connection is sufficiently low for practical use. A high-precision room-temperature wafer-level bonding technology that is useful for

high-sensitive infrared MEMS array sensor with hermetic sealing structure of the vacuum was thus established.

This chapter was concluded by the suggestion that the application of this technology is not limited to infrared MEMS array sensor, but can extend to vertical integration of MEMS devices and IC and will thus contribute to future MEMS technology evolution.

List of publications

Chapter 1

1. T.Taniguchi, R.Sato, and M.Ohba, “A study on characteristics of relay with piezo-actuator”, IEICE Technical Report, Vol.83, No.237, **7**, 1984

2. M.Sakata, K.Hosoya, and M.Ohba, “Investigation for practical use of wobble motor”, Journal of Robotics and Mechatronics, Vol.3, No.1, **47**, 1991

3. M.Ohira, Y.Koyama, F.Aita, S.Sasaki, M.Oba, T.Takahata, I.Shimoyama, and M.Kimata, “Design and Fabrication of micro mirror array for Infrared Focal Plane Array”, Proceedings of the 26th Symposium on Sensors, Micromachines & Applied Systems, **328**, 2009

4. M.Ohba, K.Kuzukawa, and K.Ozawa, “A reliability study of relay suitable for surface mount process using high-temperature-resistant plastics”, Components, Hybrids, and Manufacturing Technology, IEEE Trans. Vol.11, Issue 1, **85**, 1988

Chapter 2

5. S.Sasaki, T.Seki, M.Oba, K.Imanaka, T.Toriyama, T.Miyano, M.Kimata, and S.Sugiyama, “SNA-MEMS-Batteryless-Wireless Sensing Module Utilizing RFID”, Proceedings of the 24th Symposium on Sensors, Micromachines & Applied Systems, **433**, 2007

6. A.Kanai, M.Moriguchi, S.Sasaki, and M.Oba, “Properties of Insulator Using O_3-TEOS CVD for MEMS TSV Electrodes”, The Institute of Electronics, Information and Communication Engineers (IEICE), Vol.J92-C, No.11, **640**, 2009

7. A.Kanai, S.Sasaki, and M.Oba, “Insulator deposition on side-wall of through silicon via using O_3-TEOS CVD”, Proceedings of the 25th Symposium on Sensors, Micromachines & Applied Systems, **117**, 2008

Chapter 3

8. S.Lee, M.Moriguchi, S.Sasaki, and M.Oba, “High Aspect Through-Hole Interconnection by Electrodeposition for Vertical Integrated MEMS Device”, Electrochemical and Solid-state Science (PRiME), **2516**, 2008

9. S.Lee, S.Sato, M.Moriguchi, S.Sasaki, and M.Oba, “Mass-production Technology for Vertical Integrated MEMS”, Proceedings of International Conference on Electronics Packaging (ICEP), **596**, 2009

Chapter 4

10. M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, “Smart Bumpless Bonding for MEMS-IC Vertical Integration”, ECS Trans. Vol.16, Issue 8, **57**, 2008

11. M.Moriguchi, M.Shiozaki, S.Sasaki, and M.Oba, “Bump-less Wafer Level Bonding Experiment for Vertical Integration MEMS Device”, ECS Trans. Vol.16, Issue 8, **125**, 2008

12. M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, “Smart Bumpless Bonding for MEMS-IC Vertical Integration”, Electrochemical and Solid-state Science (PRiME), **2168**, 2008

13. M.Moriguchi, M.Shiozaki, S.Sasaki, and M.Oba, “Bumpless Wafer Level Bonding Experiment for Vertical Integration MEMS Device”, Electrochemical and Solid-state Science (PRiME), **2180**, 2008

14. Y.Koyama, M.Ohira, M.Shiozaki, S.Sasaki, and M.Oba, “Evaluation for

vacuum sealed WLP with TSV bonded by Room Temperature Bonding", Proceedings of 26th Symposium on Sensors, Micromachines & Applied Systems, **554**, 2009

15. M.Shiozaki, M.Moriguchi, S.Sasaki, and M.Oba, "Realization of MEMS-IC Vertical Integration utilizing Smart Bumpless Bonding", IEEJ Trans. Sensors and Micromechanics, Vol.130, No.5, **152**, 2010

Other publications not contained in this thesis

1. R.Sato, T.Taniguchi, and M.Ohba, "Ultra-low power consumption relay with piezo-actuator", Proceedings of National Association of Relay Manufacturers (NARM) 33rd Relay Conference, **8-1**, 1985

2. M.Ohba, Y.Nakanishi, and K.Ozawa, "Contact reliability of relay at high temperature", Proceedings of National Association of Relay Manufacturers (NARM) 35th Relay Conference, **6-1**, 1987

3. M.Ohba, K.Kuzukawa, and K.Sakairi, "Experimental study on the process of cleaning the contacts of signal control relays", Proceedings of the Thirty Fourth Meeting of the IEEE Holm Conference, Electrical Contacts, **311**, 1988

4. K.Kuzukawa and M.Ohba, "Effect of dry cleaning method for contacts of telecommunication", Proceedings of National Association of Relay Manufacturers (NARM) 37th Relay Conference, **2-1**, 1989

5. M.Sakata, K.Hosoya, M.Ohba, and M.Hirano, "Investigation for practical use of wobble motor", Proceedings of ROBOMEC 1990, Vol.1990-B, **365**, 1990

6. K.Nagahama, S.Sasaki, H,Umeda, Y.Morita, and M.Oba, “Application of Semiconductor Accelerometer for calculating velocity of a car”, Proceedings of the Institute of Electrical Engineers of Japan (IEEJ) Vol.PS-96, No.6-20, **91**, 1996

7. M.Sinohara, J.Takagi, M.Oba, and M.Takeuchi, “Curved prism array for controlling directivity of LED backlight”, Proceedings of 10th Int. Display Workshops, **665**, 2003

8. Y.Suzuki, M.Edamoto, N.Kasagi, K.Kashiwagi, Y.Morizawa, T.Yokoyama, T.Seki, and M.Oba, “Micro Electret Energy Harvesting Device with Analogue Impedance Conversion Circuit”, Proceedings of 8th Int. Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS 2008), **7**, 2008

9. M.Edamoto, Y.Suzuki, N.Kasagi, K.Kashiwagi, Y.Morizawa, T.Yokoyama, T.Seki, and M.Oba, “Low-resonant-frequency Micro Electret Generator for Energy Harvesting Application”, Proceedings of 22nd IEEE Int. Conf. MEMS, **1059**, 2009

10. T.Kawamoto, T.Yanagitani, M.Matsukawa, Y.Watanabe, Y.Mori, S.Sasaki, and M.Oba, “Large-area fabrication of $(11\bar{2}0)$ textured ZnO piezoelectric films using magnetron sputtering with linear erosion”, IEICE Technical Report, Ultrasonics, Vol.109, No.213, **65**, 2009

11. T.Kawamoto, T.Yanagitani, M.Matsukawa, Y.Watanabe, Y.Mori, S.Sasaki, and M.Oba, “Crystallographic characteristics of $(11\bar{2}0)$ textured ZnO piezoelectric films fabricated by magnetron sputtering with linear erosion”, Proceedings of Symposium on UltraSonic Electonics, Vol.30, **479**, 2009

Acknowledgments

The author would like to express his deep appreciation to Professor Kazuyuki Hirao, Department of Material Chemistry, Graduate School of Engineering, Kyoto University for his instructions that enabled him to write this doctoral thesis. Professor Hirao gave him valuable advice and advised him in the correct way to go about the writing of this thesis. The author will never forget his kindness.

The author also thanks Associate Professor Kiyotaka Miura, Department of Material Chemistry, Graduate School of Engineering, Kyoto University for his instructions and advice.

The author is grateful to Dr. Koichi Imanaka, Managing Officer and Senior General Manager of Research & Development HQ, OMRON Corporation and Dr. Sho Sasaki and Dr. Tomonori Seki, Specialists of Core Technology Center, Research & Development HQ, OMRON Corporation for their understanding, instructions, and advice.

The author is also grateful to Professor Masaaki Kimata, College of Science and Engineering, Ritsumeikan University and Professor Kaoru Shimoyama, Graduate Schools of Information, the University of Tokyo for instructions and advice concerning the development of the infrared MEMS array sensor that was the theme of this study and to Professor Susumu Sugiyama, Ritsumeikan Global Innovation Research Organization, Ritsumeikan University for his instructions and advice concerning the development of though-hole formation technology, through-hole interconnection formation technology, and wafer-level bonding technology.

Finally, the author thanks the members of Core Technology Center, Research & Development HQ, OMRON Corporation for their corporation because the author could not has accomplished the study without their help.

Part of this study was subsidized as “Development of Technology for Producing Vertically Integrated MEMS Devices”, which is popularly known

as FINE MEMS PROJECT, by the New Energy and Industrial Technology Development Organization (NEDO). The author would like to express his deep thanks to those concerned in this organization.

Masatoshi Oba